THIRD QUARTERLY REPORT
COMPATIBLE TECHNIQUES
FOR
INTEGRATED CIRCUITRY

U. S. AIR FORCE
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Period Covered
1 November 1961 to 31 January 1962

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U. S. AIR FORCE
AERONAUTICAL SYSTEMS DIVISION
WRIGHT-PATTERSON AIR FORCE BASE, OHIO

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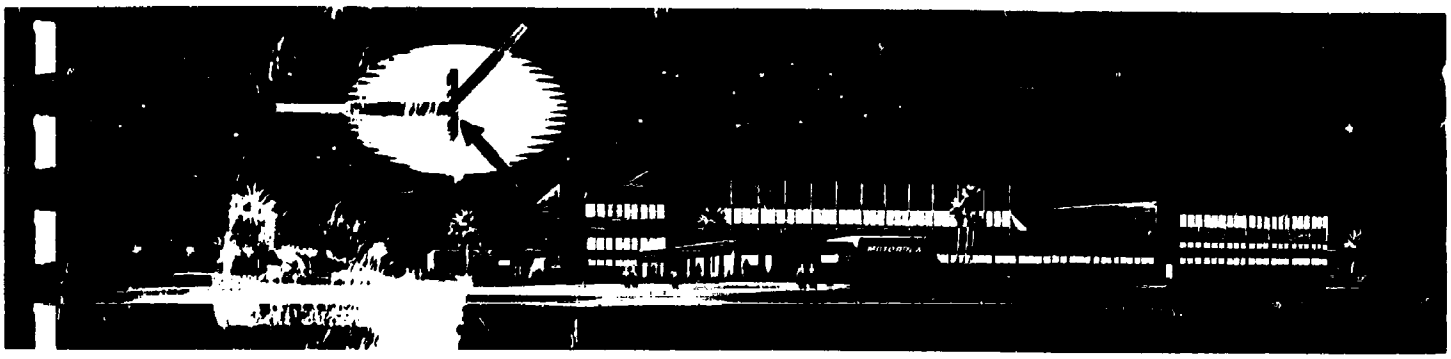

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THIRD QUARTERLY REPORT

COMPATIBLE TECHNIQUES FOR INTEGRATED CIRCUITRY

PERIOD OF

1 NOVEMBER 1961 to JANUARY 31, 1962

UNITED STATES AIR FORCE
CONTRACT NO. AF 33(616)-8276

Prepared for . . . . .

U. S. AIR FORCE
AERONAUTICAL SYSTEMS DIVISION
WRIGHT-PATTERSON AIR FORCE BASE, OHIO

Prepared by . . . . .

MOTOROLA, INC.
SEMICONDUCTOR PRODUCTS DIVISION
PHOENIX, ARIZONA

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INTRODUCTION

This report covers the second quarter's efforts in developing Compatible Techniques for Integrated Circuitry on contract AF 33(616)-8276.

Most of the effort to date has been spent in developing process techniques which are necessary for Integrated Circuit fabrication. This effort has been both in morphological areas and thin films as applied to semiconducting substrate.

Further efforts in perfecting our epitaxial techniques are reported. A program has been started to develop and fabricate typical circuits which are practical for a wide range of high and low frequency amplifier applications as well as logic circuits.

1. EPITAXIAL GROWTH TECHNOLOGY

1.1 Epitaxial Gallium Arsenide

A redesigned vacuum and gas charging system has been completed for the closed tube ampoules. The vertical furnace has been completed and is in service.

The vertical closed tube furnace has proven effective in depositing GaAs epitaxially. A new vacuum-charging apparatus is being installed.

The open tube furnace has been rebuilt and a new profile set up. Growth is still predominantly polycrystalline, however.

Additional work performed during this period was concentrated in the following areas:

1. Development of a technology for diffusing n-type impurities into gallium arsenide.
2. Epitaxial structure delineations and analyses.
3. Oxide growth on, and phosphorous diffusions into silicon.

1.1.1 Closed Tube Epitaxial GaAs

The vertical furnace described in the previous report has been used sufficiently to prove feasibility. Under temperature gradients of 40° to 50°C rather heavy deposition occurred. However, the appearance of a heavily contaminated surface indicates the necessity for obtaining a cleaner gas charge. The new charging system is being installed, therefore, on a temporary basis, until space becomes available for a permanent installation. A definite advantage to the vertical system will be the ability to measure source and substrate temperatures more accurately since the substrate attains the profile temperature of the furnace bottom rather than a local heat sink temperature as formerly.

1.1.2 Open Tube Epitaxial GaAs

A new commercial hydrogen purifier has been installed and the auxiliary purification system dismantled. This has resulted in the elimination of several glass joints and metal tube fittings which has reduced the contamination from leakage problem. The exit from the work tube has been enlarged as has the cold trap to reduce the possibility that low temperature products were recirculating to the reaction or deposition areas. This did not

appear to be a problem; however, the free exit of gasses will be maintained.

The thermal profile of the furnace indicates that the drop in gas temperature may be so severe as to cause a reversal of the reaction to take place in the flowing gas rather than on the substrate surfaces. This may well cause the polycrystalline deposition that was noted in the previous report.

An auxiliary 8 inch heating element has been installed between the present furnaces in order to obtain a more gradual temperature gradient between source and substrate. This element will be wired into the control system immediately, and the new profile obtained.

A new quartz system has been installed which is compartmented to allow separate control of the gas over the GaAs source from that entering the deposition area. With this system, hydrogen and/or HCl may be introduced into the GaAs source tube independent of the carrier gas flowing into the main deposition tube. This system allows greater flexibility in using high flows of carrier gas without sacrificing reaction efficiency between the HCl and GaAs. It will also allow a separate gas phase etch of the substrates by HCl prior to deposition.

1.2 Automatic Epitaxial Growth

A completely automated epitaxial furnace was set up. Feasibility was shown and this furnace is now in complete operation. Multi-layer structures of the N^+NP^+N and N^+NP structures were constructed for integrated circuit work. Susceptor dimensions and furnace geometry were changed to increase uniformity of growth. More heavily doped hydrogen was evaluated, and on the basis of the results obtained, was adopted.

The completely automated epitaxial furnace was set up, after some initial problems the apparatus was de-bugged and now operates perfectly.

The purge times required between layers are small for gas phase purging. However, the silicon growth on the boat is a continuous source of boron or phosphorus. Purge times between layers are kept to less than 1 minute, as the interduffusion

effect is greater than the advantage that would be obtained from a larger purge.

1.3 Silicon Epitaxial Growth Studies

1.3.1 Thickness Control

For normal device usage, a thickness control of about 10% is quite sufficient, however, for devices requiring one-micron layers, small variations in thickness of one or all of the layers can give rise to large variations in device parameters. For this reason, Motorola has been working towards a more precise control of thickness. Before attempting to modify the system in any way, close attention was paid to those variables which could affect reproducibility.

1.3.2 Temperature

The same graphite susceptor is now used on each run. Graphite screws in the back ensure intimate contact with the top quartz plate on each run. The position of the graphite in the work coil is carefully reproduced using a spacer rod. To prevent coil geometry changing either by accident or by small changes due to gravity, a more rigid 3/8" copper tubing was employed. With careful profiling reproducibility of $\pm 5°C$ can be obtained. This is approximately the reproducibility of the pyrometer so that tighter control than this is impossible using the present measuring device.

The variation in gas phase composition from run to run was checked by bubbling the H_2-$SiCl_4$ mixture through a measured quantity of 0.1 N sodium hydroxide solution and measuring the time required to neutralize the solution, using a phenolpthalene indicator. From these measurements the variation in gas phase composition was estimated at about $\pm 1\%$, over a total of 25 runs.

A baffle was placed downstream and the effect of this at various positions down the tube was checked. A slight reduction in taper down the boat was observed.

A preheater has been built and it is hoped that by heating the gas to 500 - 800°C before it reaches the reaction zone, a significant improvement will be obtained in uniformity.

Resistivity Control. Using a larger diameter tube with a larger susceptor, the resistivity variation within a run has been considerably reduced - this is aided by the use of 1% flowmeters and a completely automated system. The tightening of temperature control mentioned previously has also had a beneficial effect.

Antimony Pentachloride doped hydrogen was obtained commercially. Several runs were made but no doping effect at all was observed. The cylinder has been returned and a second one ordered. Antimony, with its far lower diffusion coefficicient could afford considerable advantages over the fast moving phosphorous presently used.

Material Supplied. Quantities of material of the $N^{+}NP^{+}$ and $N^{+}NP^{+}N^{+}$ structures have been supplied to materials research.

$P^{+}P\ N^{+}$, $P^{+}P$, $P^{+}N$, $N\ N^{+}$, and $N^{+}N$ material has been supplied to the integrated circuits group.

1.3.3 Silicon Oxide Film Thickness Measurement

Standard interferometric techniques [1] can be used to measure the thickness of an unmetallized silicon oxide film if a simple but not altogether obvious allowance is made for the film's optical properties. Suppose the oxide is removed from a portion of the area, producing a step whose height is to be measured. As is customary for gauging the height of a small step, the interferometer is set up so that the fringes cross this boundry. The step height inferred from the lateral fringe displacement across the boundry will be found to be approximately half the true film thickness. The apparent position of the glass-silicon interface for interference purposes is below its true position, and not above as it is on account of refraction in ordinary observation.

To demonstrate this fact a specimen is metallized by vapor plating. It is masked in metallizing in such a way that a boundry between masked and coated regions intersects the oxide boundary. When the interferometer centered on this intersection, it is clear that the fringes deviate in one direction in the metallized region, corresponding to a step up to the top of the oxide, and in the opposite direction in the unmetallized region,

[1] W. Bond and F. Smits, BSTJ, Sept., 1956, 1209-1221

corresponding to a smaller step down to the apparent glass-silicon interface. True oxide thickness, y, can, of course, be determined directly from the metallized region. It can be determined for an unmetallized specimen through the relation

$$y = \frac{a}{n-1} ,$$

where a is the apparent step height, and n is the index of refraction of the silicon oxide glass. The average value of n for the glass former under our conditions (1000°C in oxygen passed through a water bubbler at 50°C) was 1.47.

The experimental results are as follows:

GROWTH	a	y	n
2 hours	1000 Å	2350 Å	1.43
3	1500	3120	1.48
4	1840	3815	1.48
8	2730	5430	1.50
12	2950	6120	1.48
20	4000	8700	1.46

1.4 Oxide Growth and Diffusion Into Silicon

Work was continued on the growth of silicon dioxide films on epitaxial silicon material. This effort was in support of device fabrication studies going on in other groups within integrated circuits.

1.4.1 Gas Phase Diffusant Sources for Silicon

Conventional diffusant sources for silicon consist of borosilicate or phosphosilicate glass phases. Gas phase diffusion methods could be inherently more compatible with epitaxial silicon techniques in synthesizing integrated circuit networks. Shallow diffused junctions in silicon have been successfully produced using a mixture of diborane in hydrogen. Careful regulation of the flow rates has resulted in uniform diffusions and pit-free surfaces. Diffused junctions have been produced in p-type silicon using a mixture of phosphine and hydrogen. However, experiments to date with this system have produced pitted surfaces. It is believed that these results are due to trace impurities in the carrier gas phase.

2. THIN FILM TECHNOLOGY

2.1 Deposition of Glass Films

The purpose of this task is to develop means for depositing glass films onto semiconductor substrates utilizing technologies which are compatible with the semiconducting material and with other thin films. The films are under investigation for use as: (a) dielectric films for capacitors (b) electrical insulating films for conductor crossover insulation (c) an encapsulant for thin film components.

2.1.1 Vapor Deposited Films

Previously it had been determined that mixed glasses exhibited a higher degree of stability than do the pure metal oxide glasses. During this period the properties of alumina silicate glasses were investigated with the alumina content somewhat less than 10% and probably between 7 and 8%. In an attempt to deposit small valued capacitors to high tolerances most of this effort was devoted to the use of thick films of the order of 6000 angstrom units. With such films capacitors possessing .0015 mfd per square centimeter are constructed. Capacitors possessing 40 mmfd typically at 10 volts exhibit leakage currents of 10^{-11} amperes and dissipation factors between .3 and .4% over the frequency range from 100 cycles to 300 KC. At a frequency of 50 mc the dissipation factor rises to .66%. The noted dissipation factors were obtained with silver electrodes. The dielectric constant of this mixed glass measures to be near five.

The deposition process for the above glass films coats the entire substrate with glass. During this period photo resist techniques were developed to remove by etching glass areas not desired on the substrate. Diluted hydroflouric acid when used as an etchant completely removes a 3000 angstrom thick glass film in approximately 1 minute's time. Films as thick as 10,000 angstrom units have been deposited using mixed glass.

2.1.2 AL_2O_3 Films

Improvements were made during this month on the multiple interference equipment for the determination of film thickness. Utilizing this improved equipment the dielectric constant of

alumina films has been determined to be 9.

Reproducibility studies utilizing relatively crude dielectric film deposition equipment indicate that the tolerance of capacitors made with Al_2O_3 films can be reproduced to a tolerance of $\pm$10% at the values of 20 mmfd. Aging tests of the alumina capacitors indicate that they decrease in capacitance by a value of only 3% after 500 hours at 125°C.

Studies made of the stability of alumina film capacitors exposed to saturated water vapor at room temperature indicated in all cases an increase in dissipation factor, and in one instance, the capacitor failed due to conductor crazing. These tests indicate that in order to provide stable Al_2O_3 film capacitors protection from the atmosphere must be provided.

2.2 Silicon Monoxide Films

A series of tests were made during this month to determine the optimum electrode material for providing high Q stable silicon monoxide capacitors.

The electroding materials evaluated were (1) copper, aluminum, aluminum oxide combination in layers with the latter material next to the silicon dioxide capacitor dielectric film; and (3) copper films. Data taken after these capacitors were aged for 93 hours at 125°C show that copper backed aluminum electrodes offered the best solution for providing stable low loss capacitors. The tests utilized for this evaluation were (1) dissipation factor vs. frequency in the 1 to 100 mc range; (2) leakage current vs. voltage; (3) capacitance vs. frequency; (4) capacitance vs. temperature; (5) dissipation factor vs. temperature; (6) leakage current vs. temperature.

2.3 Tantalum Oxide Capacitors

Tantalum oxide film capacitors are being developed for use in large valued capacitors which occupy a minimum substrate area.

In general, gold films are evaporated onto the tantalum film after a portion of that film has been anodized. This desired ohmic contact has been faulty due to the thin layer of tantalum oxide which covers the tantalum electrode. During this report period, attempts were made to perfect an anodizing mask which

would prevent growth of heavy oxide layers at those points on the tantalum film to which ohmic contacts are to be made. Various waxes were applied, both from solutions and by melting, but results were unsatisfactory in that in all cases the anodization process appeared to creep under the edge of the wax covering the entire tantalum layer with an oxide film. Although electrical contact could usually be made to these areas, the contact resistances were usually high. The wax which proved to be best was Ceresin wax.

Goals were set for depositing tantalum oxide capacitors onto silicon substrates which carried an SiO_2 dielectric layer. The goals were to deposit a capacitor of 0.001 mfd on an area less than 1 millimeter square. The capacitors should have breakdown voltages in excess of 25 volts and deposited to tolerances of -50% +100%. The series resistance should be 1 ohm and the parallel resistance should be 1 megohm. It was demonstrated that these capacitors could be constructed on silicon substrate material. All goals listed above were achieved except that the series resistance was slightly over 1 ohm. This is a difficult measurement, however, it appears as though the series resistance is in the order of 1.5 to 2.5. Some of the capacitors appeared to have shorted through the substrate dielectric overlay making electrical contact to the silicon substrate. This will be studied during the next report period. Figure 2.3.1 shows tantalum capacitors on Si substrate.

Life tests have been completed on a series of capacitors which was initiated in September. The conclusions of this test are as follows:

1. The counter electrode must be pure gold. The use of chromium must be avoided.

2. A mechanical protective layer deposited on the capacitors can be silicone rubber. Hard epoxy encapsulant materials destroyed the capacitors due to strain introduced through a severe mismatch of thermal expansion.

3. The rated working voltage should be rated less than 1/2 of the anodizing potential. This voltage probably should be established at 1/4 of the anodizing potential.

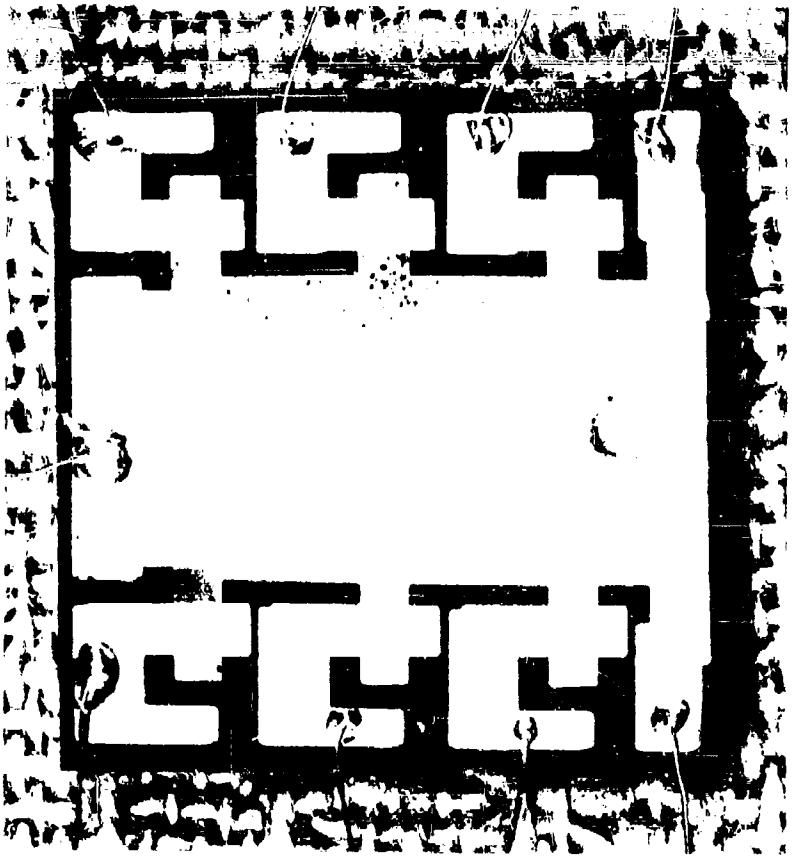


FIGURE 2.3.1

4. The 15 tantalum capacitors provided with pure gold counter electrodes and 7 with an aluminum underlay to reduce series resistance in that electrode (all anodized at 100 volts) withstood 1272 hours at 125°C, plus 9 short cycles to -55°C when 20 volts of DC was applied with no shorting failures. One shorting failure occured during the next 528 hours environmental test at 125°C with 30 volts DC applied. During the next 120 hours at 125°C with 50 volts DC applied, nine additional shorting failures occurred.

5. A problem area has been identified which involves the maintenance of excellent ohmic electrical connection between the tantalum electrode and a gold film electrical lead.

2.4 Nichrome Resistors

Improvements were made in the evaporation system to permit a better correlation in sheet resistance between the deposited films and the monitor film, and to provide a greater uniformity of the sheet resistance over a given substrate. Attempts to deposit nichrome resistor films onto silicon dioxide passivated silicon wafers to obtain 1000 ohm resistors on .05 millimeter squares to a tolerance of $\pm$5% was attempted. The tolerance of $\pm$5% was not obtainable due to several reasons which have been identified as follows:

a. Lack of uniformity of film deposition which has been corrected as described above.

b. Lack of uniformity of the deposition mask which has been traceable to deviations in the original art work.

c. The nichrome resistor films appeared to be shorting through the glass dielectric overlay to the underlying silicons.

These effects have been studied during this period and means have been sought to eliminate them.

The temperature coefficient of films deposited at 100 ohms per square sheet resistance are quite close to that of the bulk nichrome material and have ranged between 75 and 90 ppm/°C. Aging tests continued during this period with continued excellent results. The majority of the films aged around 500 hours at 200°C have indicated a change in resistance of less than 1%.

Nichrome film resistors are being evaluated for use as relatively low valued thin film resistors on silicon substrates. The incorporation of modifications in the evaporation facility enabled the agreement between the deposition monitor and films deposited within a square 4 inches on the side to be within a tolerance of $\pm$5%.

Also during this period an automatic monitor system which operates a vapor stream shutter has been devised and incorporated into the evaporation equipment. Utilizing this equipment a predetermined resistance of the monitor can be achieved to values closer than $\pm$1%.

Temperature coefficient resistivity measurements on films deposited on glazed ceramics possessing sheet resistance values of 300 ohms per square all exhibit less than -30 ppm/°C.

Experiments have been initiated during this period to determine the maximum number of evaporations possible for a one-sample source material before a change in film properties due to selective evaporation of the nickel-chromium constituents can be detected.

2.5 Spiral Inductors

The study of spiral inductors deposited onto passive silicon substrates continued during this period. In one test a 300 ohm-cm sample of silicon was utilized which possessed a 1.5 micron thick insulating overlay of grown silicon dioxide. Two twenty turn inductor coils were deposited onto this sample and the inductance and Q values measured for these coils were taken at frequencies ranging from 15 mc to 100 mc. The inductance values agreed closely with those measured on the 50 ohm-cm material as reported in the last monthly report. However, the Q values were greatly enhanced and appeared to be about one half of that of similar coils deposited on glass substrates.

A second experiment was performed utilizing 300 ohm-cm samples of silicon with overlay dielectric thicknesses of 0.5, 1.0, 1.5, and 2 microns. Twenty turn spiral inductors were fabricated on these samples to determine the effect of variation in dielectric thickness on the Q values. The Q thickness vari-

ation over these small ranges is not significant in changing the loss mechanisms introduced by the conducting substrate. Figure 2.5.1 shows thin film spiral inductor on Si substrate.

The conclusions obtained to date on this study are:

1. A minimum resistivity of 50 ohm-cm is required to obtain measurable values.

2. Fifty ohm-cm and preferably 300 ohm-cm silicon is required to obtain appreciable Q values. The latter substrate provides inductors with Q values approximately one and one half that of inductors deposited on glass substrates.

3. The insulating overlay on the semiconductor should be at lease 1.5 microns thick.

4. The optimum frequency for the inductor utilized in this test appears to be between 20 and 50 mc.

2.6 Combined Thin Film Components

A program was initiated during this period to determine means for utilizing combined thin film inductors and capacitors for tuned circuits within the frequency range of 10 mc to several hundred mc.

The work done during this period utilized a 20 turn flat spiral inductor possessing a conductor width of .003", a conductor spacing of .003" and a conductor thickness of approximately .001". The outside diameter is .330" and the inductance is 2 microhenries. Tuned circuits utilizing this coil and silicon monoxide thin film capacitors were made which possessed overall Q values in the range of 15 to 20 at a frequency of 10 mc.

Three methods of adjusting the resonant frequency of such a circuit were investigated. One of these involved incremental adjustments of the capacitor by disconnecting small capacity fingers built into the capacitor. This method offers a possibility of tuning over a wide frequency range. The method is permanent. In practice, a large capacitance is constructed and then the tuned circuit is adjusted to frequency by removing the correct number of tuning fingers built into the geometry of the capacitor. This is done by cutting away the top electrode.

A second means investigated for tuning this LC combination

FIGURE 2.5.1

involved adding distributed capacitance across the inductor by adjusting the spacing between the inductor and a grounded metallic plane. Figure 2.6.1 shows the percent of detuning available by this method.

Both aluminum and copper metal discs were utilized and the disc diameter was identical to that of the diameter of the inductor. The metal planes were .300" in thickness.

A third method for tuning the LC circuit investigated utilized a magnetic paint which is applied to the spiral inductor to increase its inductance value. In the initial investigations the spiral inductor was covered with protective coating approximately .015" thick. When ferrite magnetic paint was applied directly onto this coating (the magnetic coating was about .010" thick), a change in resonant frequency was observed from 10 mc to 9.5 mc.

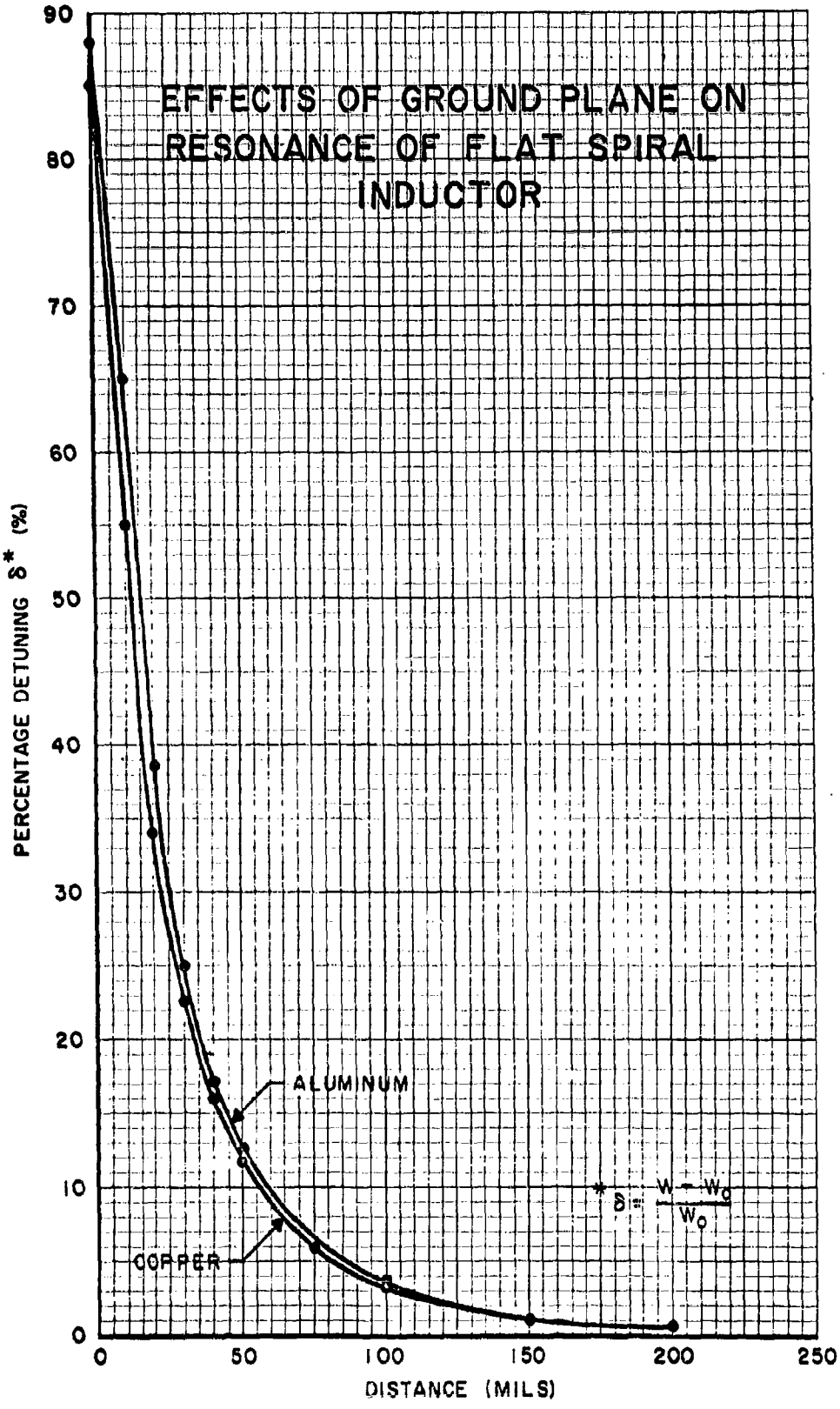

EFFECTS OF GROUND PLANE ON RESONANCE OF FLAT SPIRAL INDUCTOR
PERCENTAGE DETUNING δ* (%)
90
80
70
60
50
40
30
20
10
0
0
50
100
150
200
250
DISTANCE (MILS)
ALUMINUM
COPPER
* δ = (W − W0) / W0

FIGURE 2.6.1

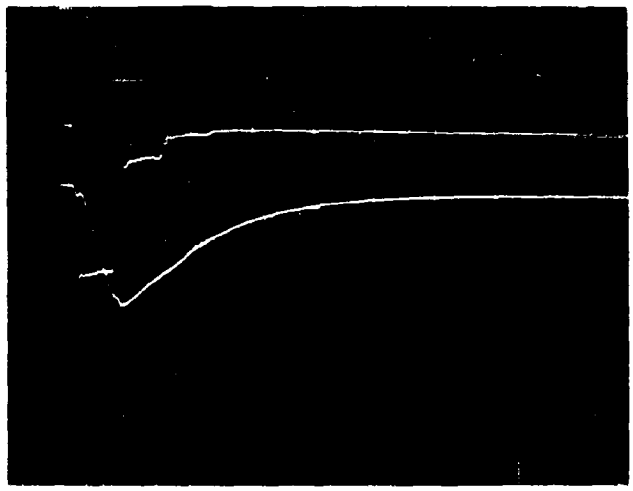


FIGURE 3.1.1

3. SEMICONDUCTOR TECHNOLOGY

3.1 Diffused Resistors

Frequency Response - Figure 3.1.1 indicates the pulse response of a 30K diffused resistor, when connected as a three-terminal device. The 30 K ohm resistor was obtained from the total series of 110 squares and had a junction capacitance of approximately 25 pf. This unit exhibited a 3 db break point of about 100 kc.

The 300 ohm resistor has a better pulse response although it has the same parasitic junction capacitance. Resistors made up from a small number of squares should have good frequency response beyond 100 Mc.

Junction Capacitance - The capacitance of the P-N junction of the diffused resistor was measured as a function of the reverse bias voltage across the junction. Figure 3.1.2 indicates the measuring circuit and the resultant curve. The values of this curve closely follow the theoretical form for a reverse biased junction of

$$C = KV^{-1/3}$$

where, for this unit, $K = 18.5 \times 10^{-12}$.

The values of capacitance as shown above are for the total 110 squares of a typical 30 K ohm resistor. Lower values of resistance would have lower values of junction capacitance.

Pulse Delay - A 30 K ohm diffused resistor was connected in the following circuit for pulse delay measurements.

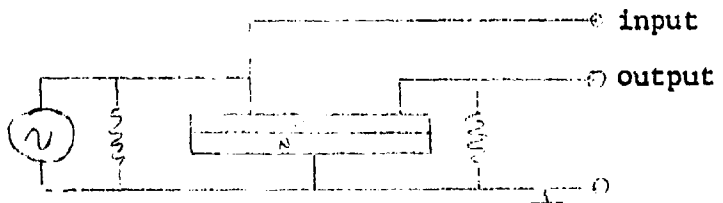


Figure 3.1.2

A negative 5 volts 350 nsec pulse was applied to the input. The figure illustrates the pulse delay time through series of 110 squares of the diffused resistor. The delay time to the 50% point of the output was approximately 200 nsec. The delay time was not measurable for a single square of the unit.

Temperature Coefficient. Measurements are now being made to determine the temperature coefficient of the boron diffused type resistor. It is planned to obtain curves over the range of -60°C to +150°C for various units.

3.2 Silicon Dioxide Capacitors

Capacitors with large values of capacitance per unit area are being made by metallizing over very thin layers of silicon dioxide on a silicon substrate. One method uses a thermal oxide which is produced by the high temperature oxidation of the silicon substrate developing an oxide approximately 1000 Angstroms in thickness. This oxide is then metallized with an aluminum layer which is then bonded to the oxide by a subsequent temperature treatment. Devices of this particular structure are being studied to determine their initial characteristics and behavior under long term stress conditions.

These devices show a very low bulk leakage current at modest voltages consistent with the bulk resistability properties of silica which is the structure of the thermal oxide.

Departure from this nearly ideal behavior is noted as higher voltages are applied. If the voltage is increased in a low impedance test circuit the capacitors can fail by the formation of a short between the silicon electrode and the aluminum electrode. This is a conduction path through extremely small isolated regions of the very thin oxide dielectric.

Close examination of these types of failures show that the small failure regions are not random in their location, but usually follow line patterns or area patterns. Microscopic examination of capacitors with the aluminum electrode removed indicate that the failure occurs in regions where the oxide is either not thick enough to sustain the applied voltage or else is not uniform in thickness. One type of non-uniformity appears as lines in the

oxidized structure, possibly due to scratches on the substrate silicon.

Measurements have been made of the surface profiles of wafers prior to growth of the oxide dielectric using an interference microscope. Surface irregularities exist in the base wafer. Although some of these irregularities are probably of little consequence when a thick oxide is thermally grown, such as a 10,000 Angstrom layer used for a diffusion mask in transistor fabrication, they may represent a considerable perturbance in a 1000 Angstrom structure.

The oxide growth takes place on a silicon surface having a very thin "native" oxide already present. The "native" oxide may vary in thickness from less than 100 Angstroms to a few hundred Anstroms, depending on the previous handling and history of the wafer. Studies are being made of stabilizing surface treatments prior to oxidation to ensure better uniformity of oxide growth and dielectric properties. The handling procedures through the critical cleaning, oxidation and metallizing steps will be studied.

Some capacitors have been made which show a stable avalanche type breakdown at voltages near the known values for maximum field in silica. Operation of capacitors at higher voltages (without decrease in capacitance per unit area) will be possible as the structure of the oxide is made more uniform.

The effect of the metallizing processes can also contribute to unit reproducibility and reliability. Optimum thermal treatment will be determined in order to produce tight bonding of the aluminum to the oxide with the least perturbation of oxide thickness, which can occur by reduction of the oxide at higher temperatures. Breakdown has produced visible changes in the appearance of the metallized layer. This tool is also being used to study the structure of the capacitors.

3.2.1 Forced Failure of Capacitors

The attached microphotographs show examples of capacitors which were forced into failure by application of short voltage transients at succeedingly higher voltages. Voltages up to 150

volts were applied, in steps, causing breakdown to occur sequentially from regions of lowest breakdown to highest. In some cases this process can be carried until an "avalanche-like" current of a few microamperes can be sustained continuously.

Figure 3.2.1.1 shows the top surface of a capacitor with the aluminum still on the surface. The dark region at (a) is the location of contact of a probe with the aluminum. Prior to application of voltage, the circular aluminum contacts of all the capacitors were free of spots and lines. As the voltage was increased on this unit, a dark line started to appear at the top center of the aluminum circumference and progressed downward across the aluminum region. The voltage was removed and the photograph taken before the line was pushed all the way across the pellet. Close examination shows a small line or crack in the unmetallized surface at the end of the track on the aluminum. The tract is curved, discontinuous, and looks wider at the initiating end than at the point where it ended.

Figure 3.2.1.2 shows two capacitors adjacent to each other on a single wafer. The capacitor on the left was stressed to a higher voltage than the one on the right. A greater density of spots has been produced on the left hand unit, with an especially large density at the bottom of the picture. The right hand unit has developed a fairly broad line across the upper right corner of the photograph. Both units show an array of spots falling on a line running from top left to lower right, just below and parallel to the line of the microscope reticle.

Figures 3.2.1.3 and 4 show two more capacitors which were etched after forced failure. First the units were etched with an etch which attacked exposed silicon dioxide, then with an aluminum etch, and then a partial etch of the silicon dioxide exposed under the removed aluminum. On both of these units the line patterns are clearly visible. (The large spots on both are the regions where probe contacts were made.) The angles between the line patterns do not appear to have any correlation with the crystallographic orientation of the silicon.

The three figures 3.2.1.5 A, B and C show a single capa-

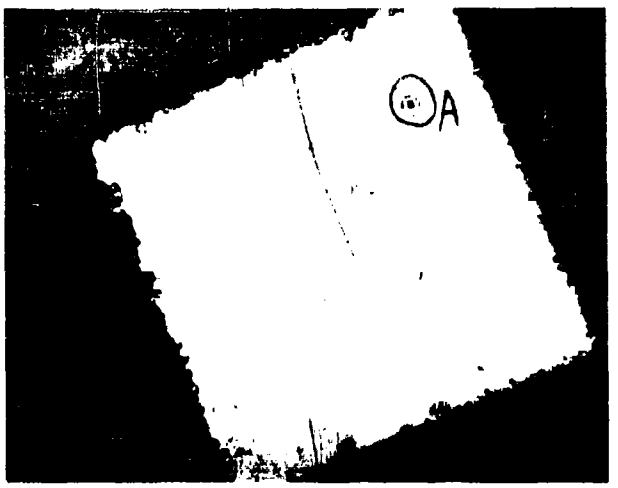


FIGURE 3.2.1.1

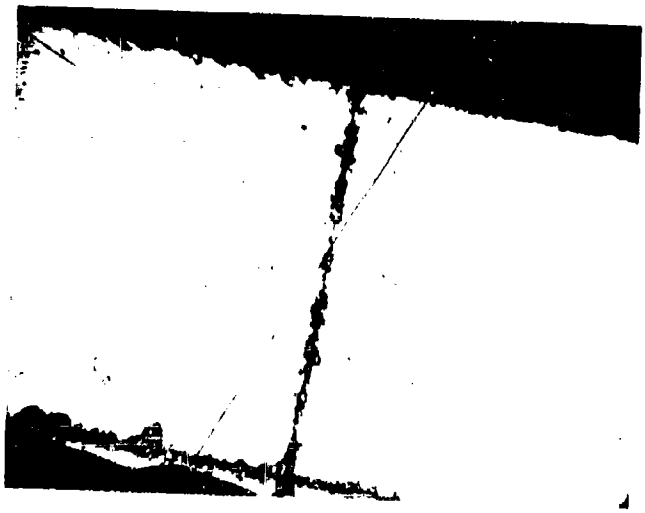


FIGURE 3.2.1.2

FIGURE 3.2.1.3

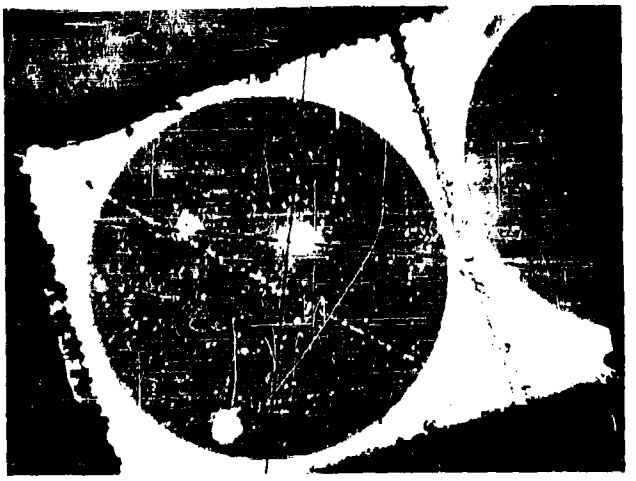


FIGURE 3.2.1.4

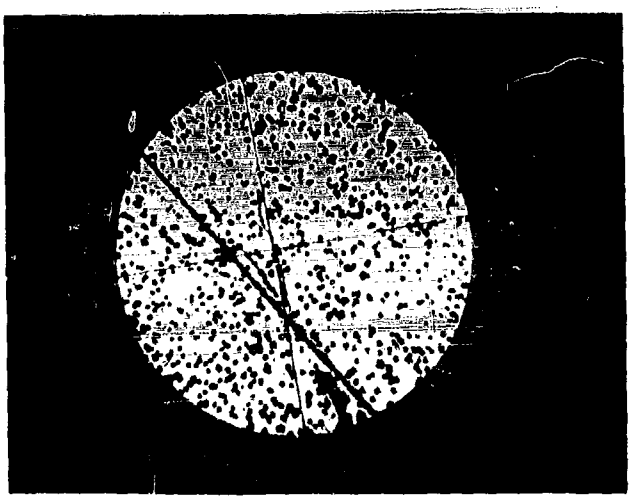


FIGURE 3.2.1.5A

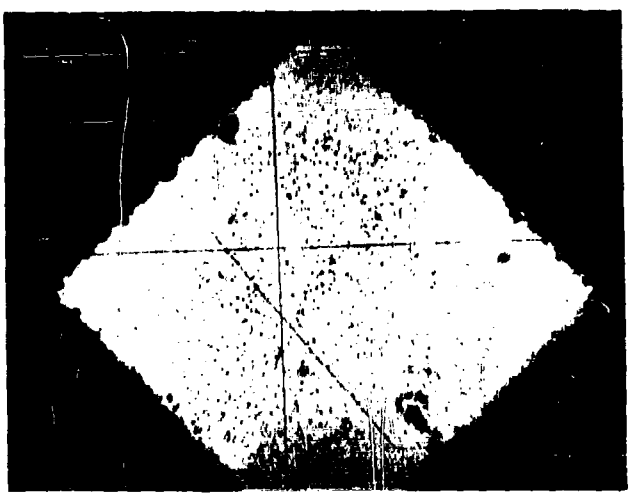


FIGURE 3.2.1.5B

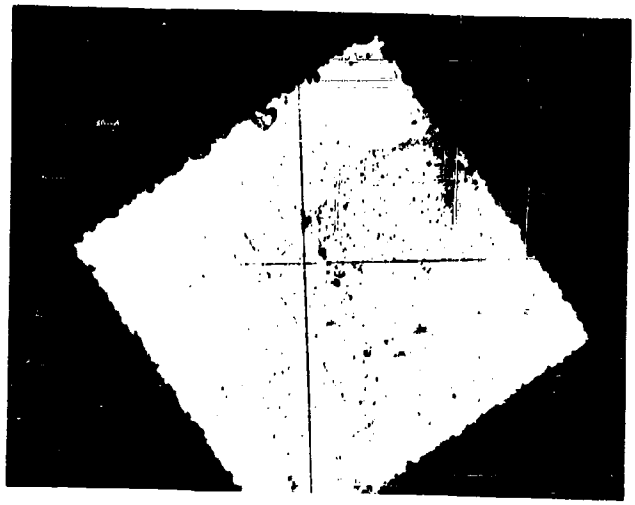


FIGURE 3.2.1.5C

citor. 5A is the capacitor with the aluminum still on it. 5B shows it after the aluminum has been removed; the pattern can still be seen in the oxide, although the spots are smaller in size. This indicates that the oxide dielectric failed in small regions but the alumina electrode has been distrubed in somewhat larger regions about each failure spot. 5C shows the same unit after removal of all the silicon dioxide. The silicon shows the same pattern as was seen in the oxide and in the alumina.

The distribution of spots stops at the edge of the aluminum contact and in none of the three do they show outside the original metallized circle. They are not present until after a unit has been forced to fail.

Model of Failure Process. A model can be constructed describing what happens at one of the failure spots. As the dielectric strength of a small region is exceeded the localized concentration of current causes the aluminum upper electrode to alloy with the silicon through the silicon dioxide dielectric. In most cases, under suitable circuit conditions, a small region of aluminum on the surface surrounding the initial spot is ruptured or dissolved away into the alloying region, breaking the electrical continuity of the rest of the aluminum surface with the alloyed spot. Since the current is supplied from the probe contact through the surrounding surface layer of aluminum to the small region of dielectric breakdown, this breaking of the continuity causes the process to stop at this point, and as the supply voltage rises slightly, to start at the next weakest or narrowest point in the oxide dielectric.

Some other characteristics also fit this model. The capacitance of a unit decreases monotonically as it is forced into failure at more and more spots. This is a result of the smaller electrically continuous area of aluminum available. If the forced failure is carried out under electrical conditions which allow the localized spot to form without completely breaking the electrical continuity of the aluminum the capacitor has an electrical characteristic similar to that which occurs when a very small aluminum alloyed region is made on low resistivity N-type silicon.

3.3 Isolation of Active Elements in a Single Block of Semiconductor Material.

As discussed earlier, the method proposed for isolating active elements within a single block of silicon is based upon the high impedance of two P-N junctions back-to-back, with both junctions reverse-biased or left floating. The DC impedance of silicon planar junctions is quite high, even at temperatures approaching 150°C. The impedance at high frequencies is dependent upon junction capacitance, which is determined primarily by junction area and the impurity concentrations on both sides of the junction. However, since this parasitic junction capacitance is an inescapable feature of this system, the area of investigation has centered around the basic problem of achieving an acceptable level of DC isolation.

There are three methods of forming this type of junction isolation under evaluation and these methods will be discussed in some detail.

A particular type of NPN silicon transistor structure is under evaluation for use in each scheme. The transistor is designed to have f_T in the 600 - 800 mc range, with an h_{fe} peak around 1mA. The junction capacitance of the collector-base diode is designed around 2pf. These units have top collector contacts to facilitate interconnection between elements and because collectors must necessarily be contacted at the top surface in two of these geometries.

Data is included showing gain-bandwidth product versus collector current. These units were fabricated using the planar structure and did not involve top collector contacts, but were made from N N + epitaxial silicon material so that a comparison may be made between this conventional unit and the top collector contact unit. Initial studies of top collector contact 2N834 units indicate a 10 millivolt drop between the substrate and the top surface contact at a current of 1mA. The 2N834 is a planar NN+ epitaxial transistor similar to the new VHF transistor under evaluation. Figure 3.3.1 illustrates the cross sectional structure of this new transistor as it will be used in a typical inte-

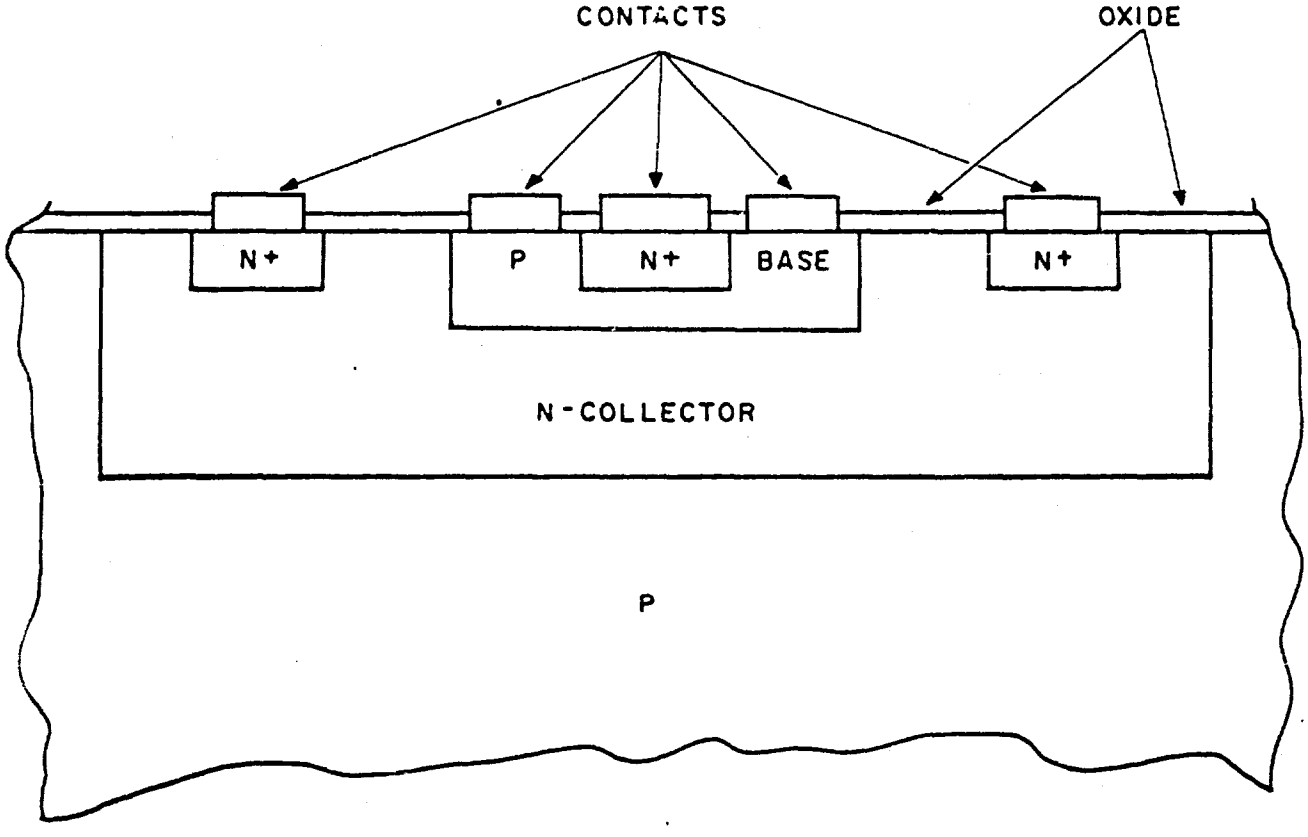


FIGURE 3.3.1

STRUCTURE OF PLANAR TRANSISTOR USED IN ISOLATED COLLECTOR ANALYSIS

grated circuit.

Each of the methods under evaluation is basically a 4-layer semiconductor device. Two methods have all planar junctions, while the other does not. To avoid the effects of a 4-layer device (such as a controlled rectifier) the width of the N-type collector region is designed to be much greater than the diffusion length of carriers in the collector. Lifetime killing techniques and a wide collector region will assist in avoiding this particular parasitic.

The first method of junction isolation is illustrated in Figures 3.3.2A and 2B. N-type starting material has a series of interconnecting "wells" of P-type impurity diffused completely through the slab. The structures to be isolated (transistors, diodes, diffused resistors) are then diffused into the islands of N-type material.

Advantages of this structure are:

1. The N-type region, in which the active devices will be fabricated, is single resistivity silicon, rather than a region with an impurity gradient.

2. There is no requirement for a low surface concentration N-type diffusion.

Disadvantages of the structure are:

1. The width of the diffused P-type channel will be greater than the final thickness of the wafer itself. As a result, the isolating junction will occupy large areas.

2. The P-type diffusion will require many hours to diffuse through a silicon wafer as thin as .003" - .003".

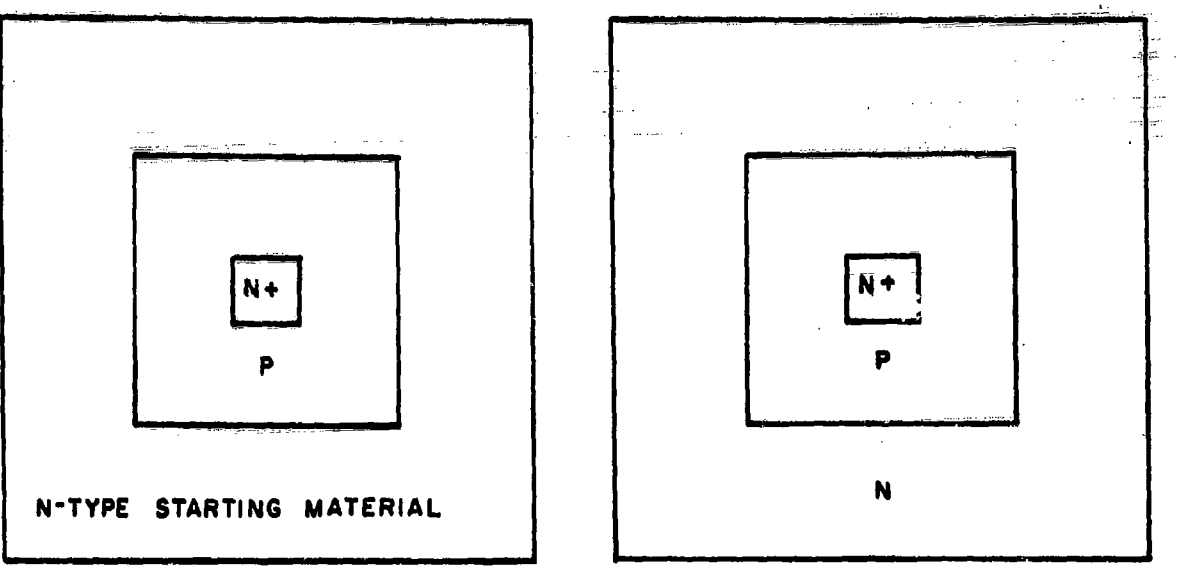
The second method of junction isolation is illustrated in Figures 3.3.3A and 3B. This method consists of diffusing successive NPN= regions into P-type starting material.

The advantages of this type of structure are:

1. The junctions are all planar.

2. The area consumed by the P-type channel may be held to a minimum.

The disadvantages of the structure are:



P-REGION DIFFUSED THROUGH
N-TYPE WAFER

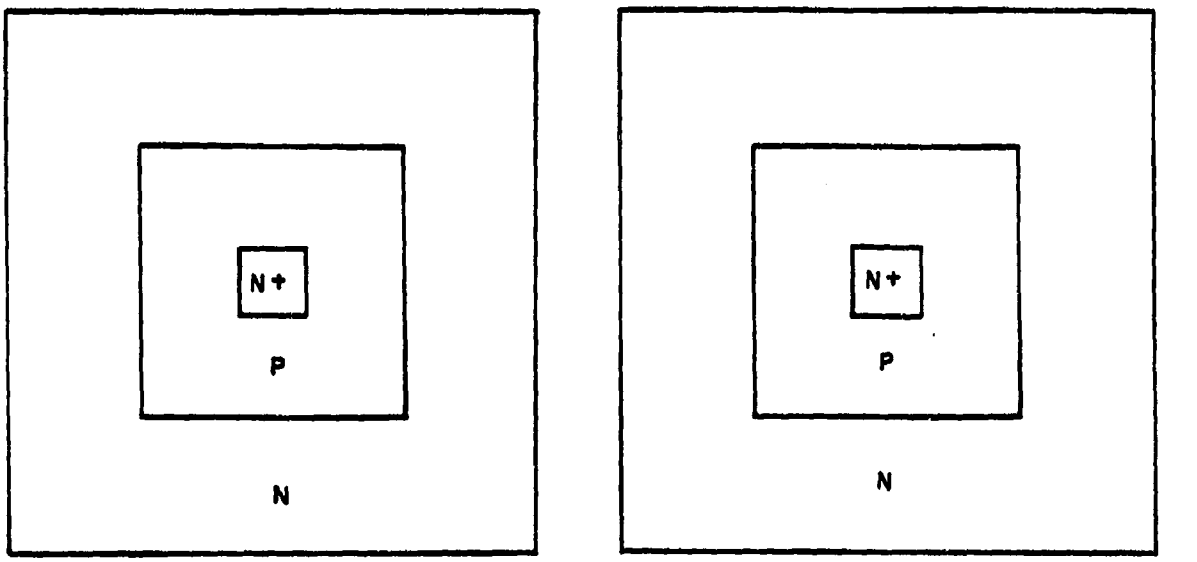


FIGURE 3.3.2A

GEOMETRY OF SYSTEM USING P-TYPE DIFFUSION THROUGH N-TYPE WAFER

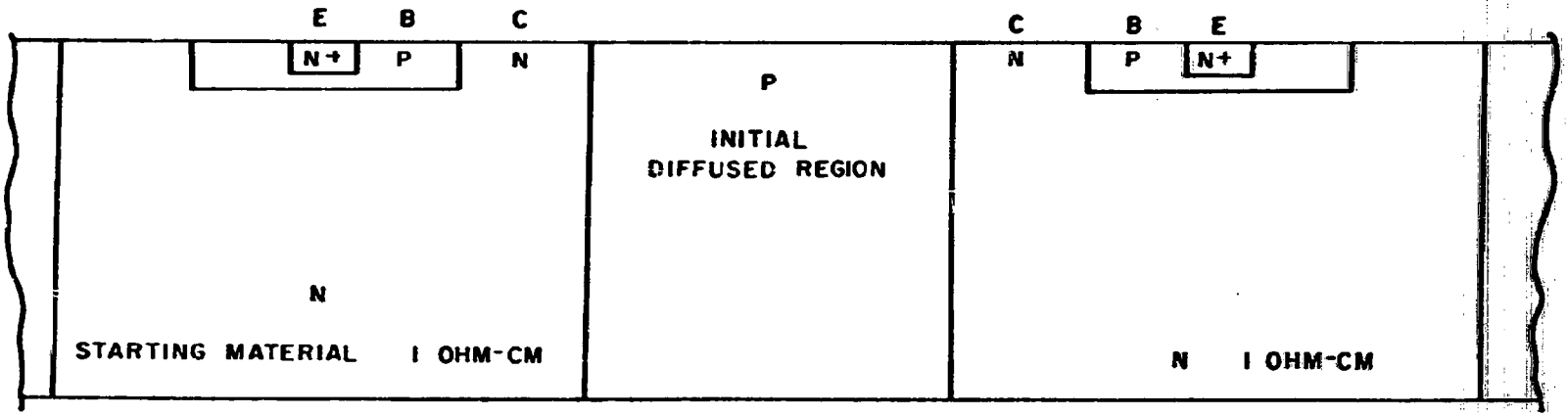


FIGURE 3.3.2B

CROSS SECTIONAL VIEW OF STRUCTURE SHOWING P-DIFFUSION THROUGH AN N-TYPE WAFER

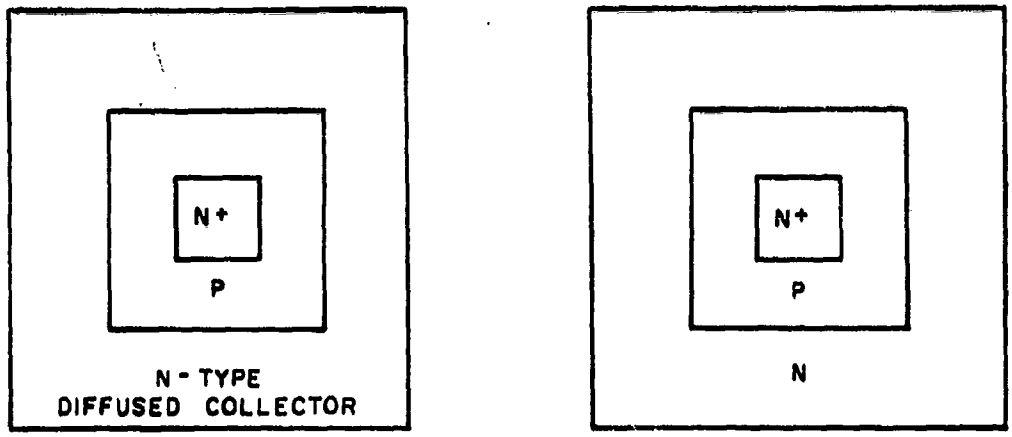


FIGURE 3.3.3A

GEOMETRY OF JUNCTION-ISOLATED COLLECTOR REGION

USING TRIPLE DIFFUSION

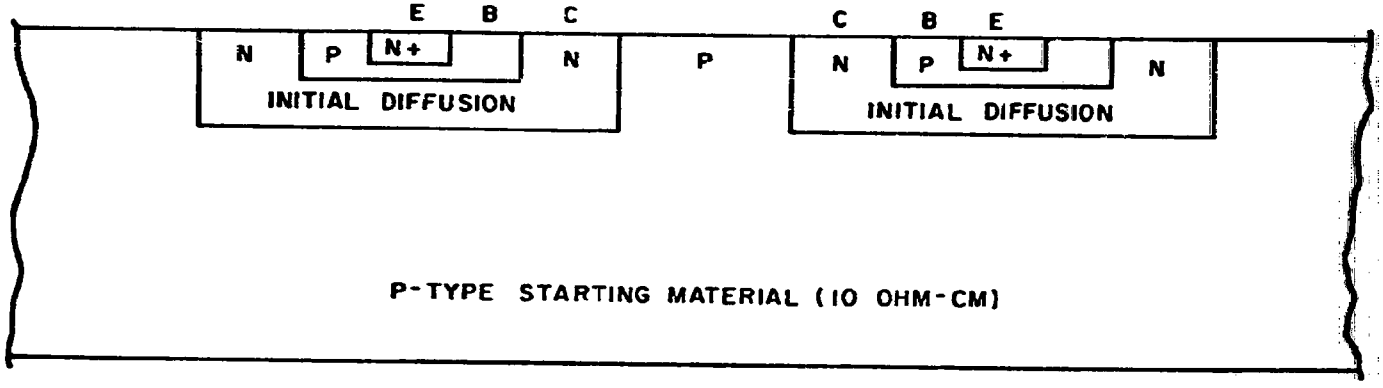


FIGURE 3.3.3B

CROSS SECTIONAL VIEW OF JUNCTION-ISOLATED COLLECTORS FORMED BY TRIPLE DIFFUSION

1. A low surface concentration N-type planar diffusion is required. Problems in controlling the surface concentration of N-type diffusion and maintaining a low reverse leakage diode have been encountered.

2. The N-type region in which the active devices will be formed has an impurity gradient across the region.

The third type of structure is illustrated in Figures 3.3.4A and 4B. This method is very similar to that described first. A wafer of P-type silicon has a layer of N-type silicon epitaxially grown upon it. A P-type channel is diffused through the N-type region to the original P-type silicon. The final structure is similar to the triple-diffused geometry, but the method used for forming N-type regions isolated by P-type channels is similar to method one.

The advantages and disadvantages of this structure are similar to those set forth with method one, with one exception. The N-type region may be considerably thinner than an entire N-type silicon wafer, and the time to diffuse through the N-type epitaxial region will be substantially less than that required to diffuse through a wafer .003" to .004" wafer.

All three methods are under investigation, and N-type regions have been successfully formed by method two. Epitaxially grown junctions have been evaluated prior to diffusion of the P-type channel, and these junctions have shown sufficiently low reverse current to be useful for DC isolation.

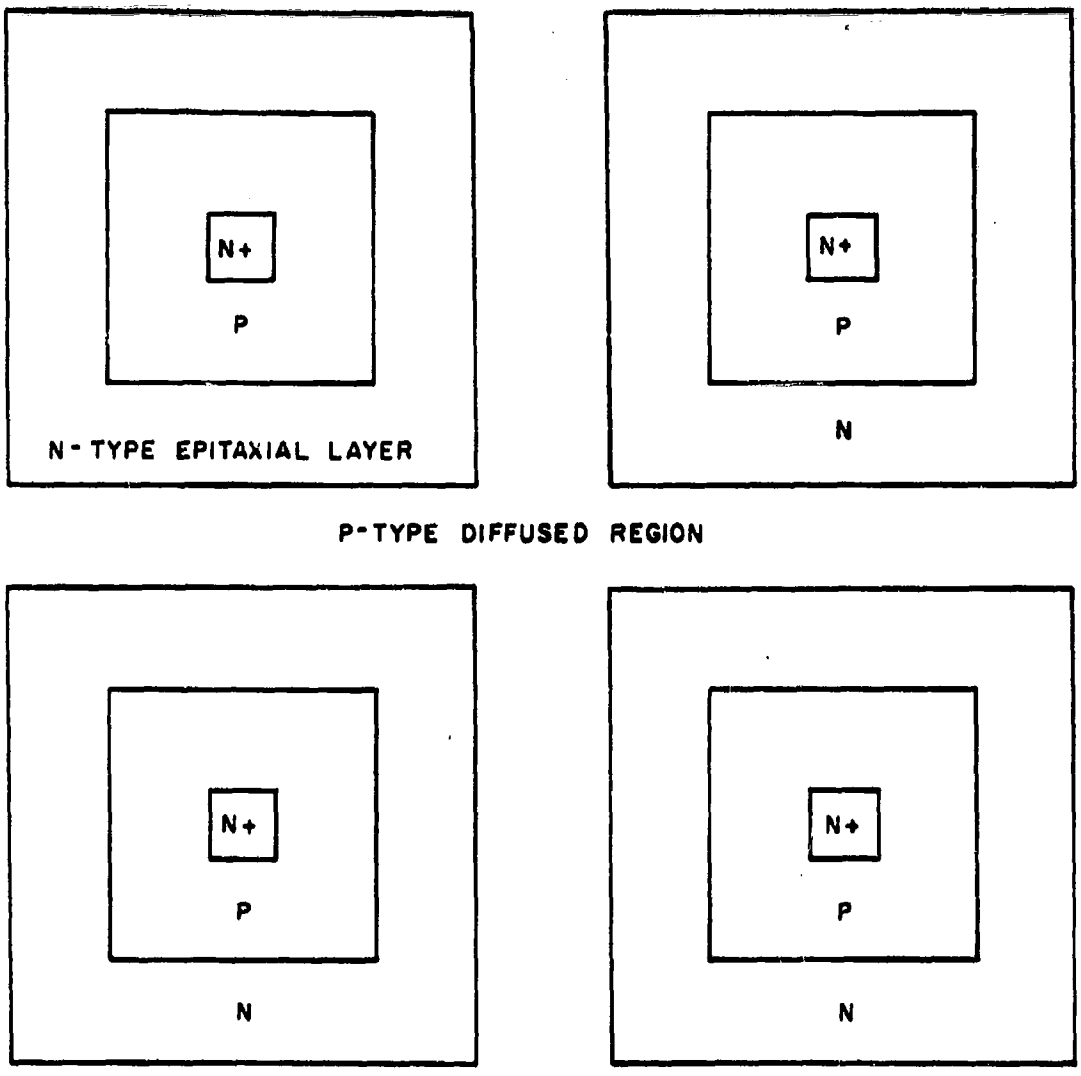


FIGURE 3.3.4 A

GEOMETRY OF JUNCTION-ISOLATED COLLECTOR REGIONS FORMED

BY PLANAR-EPITAXIAL PROCESS

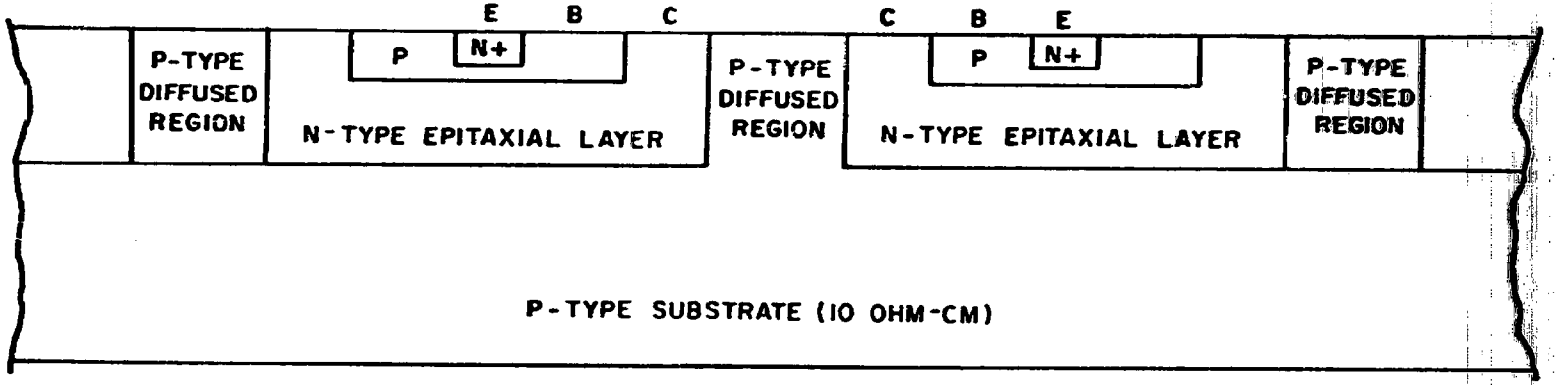


FIGURE 3.3.4B

CROSS SECTIONAL VIEW OF JUNCTION-ISOLATED COLLECTOR REGIONS FORMED BY PLANAR-EPITAXIAL PROCESS

4. CERAMIC & FABRICATION TECHNOLOGY

4.1 Mask Design

Several masks sets have been designed for use in building both components for Integrated Circuit use and Integrated Circuits themselves. There are four basic considerations involved in designing any photomask:

1) Tolerances on the pattern.
2) Spacing of the pattern.
3) Resolution of the pattern on the photographic plate.
4) Parasitics between structures.

4.1.1 Tolerances

Etched patterns with a 0.0003" line width have proven to be reproducible. The diffused resistor pattern involves etching a line with a minimum thickness of 0.0005", and the inductor pattern has a minimum line width of 0.0003". Tolerances down to $\pm$0.0001" certainly do not seem impractical at this time.

4.1.2 Spacing

Patterns are generally spaced on 0.025" centers or on multiples or 0.025".

4.1.3 Resolution

Patterns have been resolved on the photographic plates commonly in use which are about an order of magnitude smaller than are practically useful at this time. Hence, the state-of-the-art in micro-photography is not limiting to semiconductor technology.

4.1.4 Parasitics

The most common parasitic involved is that of spurious capacitance. Regardless of the scheme employed for isolating collectors in a single piece of semiconductor material, there is an inescapable parasitic capacitance. As mentioned in previous reports, a method has been devised to fabricate two transistors in a single slab. A mask has to fabricate two transistors in a single slab. A mask has been designed for placing two isolated transistors and two isolated resistors

(diffused) on a single slab. Parasitics primarily to be studied are the capacitance and the finite resistance between structures.

Another area of interest is redundancy. With an excess of diodes available, studies will be performed as to the effect on yield of having extra units available for bonding after testing.

4.2 Packaging

A general review of packaging technology has been performed during the last reporting period. Experiments indicate that the ceramic and contact technology is applicable to either the round or rectangular figure. Considerable effort is spent in layout to eliminate the thermal compression wire bonding and/or to reduce the length of the bonded wire.

4.3 Metallization

Photoresist techniques for selectively removing metallization from ceramics has been developed and lines down to 10 mils have been etched.

The process consists of processing a ceramic disc with moly-manganese metallizing on both flats, then a photo sensitive emulsion is coated onto the ceramic, and a circuit is exposed on the emulsion by means of a glass mask. The unexposed emulsion is then washed away in development.

The excess metallization is now ready to be removed by a chemical etch while the circuit remains protected by the photo-resist emulsion.

Various thicknesses of gold can then be fired onto the circuit and experiments are underway to determine the best thickness to give maximum bonding of the silicon chips to the circuit on the ceramic.

By this process many thermal compression wire bonds are eliminated and the circuit is such that eutectic solder bonds can be made directly to the edge of the ceramic disc.

This will mean that complete circuits will be processed and tested before encapsulation or before the completed circuit is bonded to the header.

Photoresist processes have been developed for chemically etching selective circuit patterns on metallized ceramic discs.

The process consists at the present of two different techniques both of which will give versatility in the patterns on the ceramic.

The basic ceramic consists of a high density alumina (94%) which has been pressed and cured into a specific shape.

There is also provided a scaled crosshatch for relative location of metallizated areas. The lines in the crosshatch are blue, and will not reproduce in the final mask negative.

The desired pattern can then be drawn in using india ink or black wax pencil, either free hand or using straight edge guides. This template is photographed at 10:1 scale reduction, producing a single glass mask ready for ceramic exposure in about 20 minutes elapsed time.

4.4 DIE BONDING

Many tests have been run on the effectiveness of die bonding of silicon chips to this metallization. All evidence so far indicates that the wetting is excellent and the bonds obtained very satisfactory. One interesting phenomenon is a marked whitening of the gold layer which has been ascribed to absorption of the excess gold in a nickel gold eutectic. This may play an appreciable part in the bonding efficiency since the absorption of excess gold results in a stronger bond.

4.5 FABRICATION FACILITIES

Patterns of metallization are obtained in the homogeneous composite layer by a combination of photoresist and etching. A high contrast photo mask is first prepared which includes the pin contacts, bonding islands, and substrate electrical interconnections.

The metallized ceramic, previously coated with a suitable photoresist material is exposed, developed, and etched in Aqua Regia.

Adequate etching experiments to prove-in optimum conditions have up to this writing been somewhat restricted because of short supply of the ceramic wafers. Since now deliveries of these are coming in, the etching process can be rapidly perfected.

Tentatively, it appears KPL resist is the most useful medium, and adequate patterns for many relatively simple configurations can be obtained, even with some slight roughness in edge definition and slight undercutting.

Techniques for making ceramic etching masks with a minimum of time delay have been developed. For a mask to expose single wafers, which may be useful in the evaluation of a limited number of circuits, art work for the photography may be generated from scaled engineering drawings by conventional methods. In cases where the location tolerances are not critical, hand drawn masters can sometimes be used. To facilitate this operation, a master drawing at ten times scale has been prepared. This indicates the scallop orientation, contains an outer ring for visual centering, and indicates metallization areas in the vicinity of the pin, for pin bonding.

4.6 POST BONDING

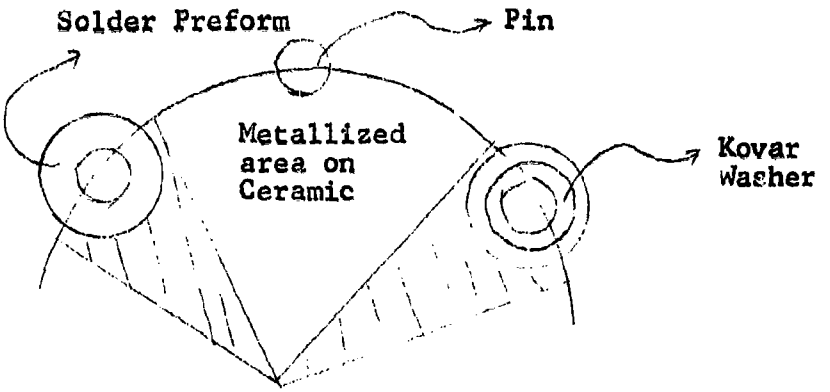
The metallized terminal segments formed as part of the circuit on the ceramic wafers, must be bonded to the header posts both for electrical contact and, in the case of multiple layer stacks, for mechanical support also.

There are several attractive approaches which meet the requirements technically, but there are distinct advantages of some of these over others in ultimate assembly cost.

The most immediately available technique consists in applying over each post where a bond is required a preform gold-germanium washer which contacts with the gold metallization on the ceramic, and closely fits the header post.

When this part is subsequently melted down, it should flow in on both parts and bridge the few thousands of an inch gap.

A somewhat more reliable approach appears in adding a second washer of some metal which wets well, such as kovar, over the solder preform. This assembly assures more reliably that the gap will bridge. These alternate assemblies are sketched herewith.



This is a hand assembly operation which should ultimately be replaced with a lower cost method. Several approaches are being considered, some of which involve multi-preforms, wire spiders, edge metallized ceramic wafers, pre-bonded metal loaded washers, etc.

5. INTEGRATED CIRCUIT TECHNOLOGY

5.1 Integrated Circuit Design

The procedure for integrated circuit design is most easily understood if it is broken down into several steps. The steps are;

1. Conventional circuit design.
2. Adaptation of conventional design to integrated circuits by use of integrated circuit elements in separate packages.
3. Single package fabrication and test
4. Final fabrication into integrated circuit form.

The conventional circuit design requires no discussion. The adaptation to integrated circuits must follow new ground rules and these should be discussed in detail. A summary chart of these rules is provided for ready reference. The rules are subject to considerable revision as the integrated circuit art develops.

ELEMENTS FOR INTEGRATED CIRCUITS

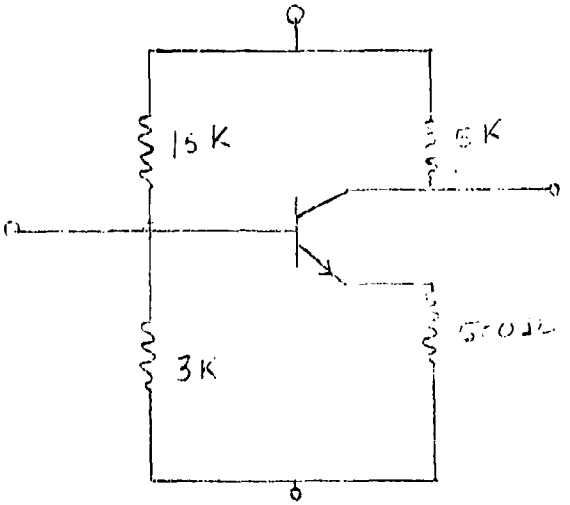
Element Function	Type	Range	Current Voltage or Power	Temperature Coefficient	Tol.
Resistance	Diffused N or P	10 to 100K 300 - 30K prefer	1/2 watt 1/4 watt suggest	(Varies with doping.)	±10% ±1% ratio
Resistance	Tin Oxide SnO_2	1K to 10meg	1/4 watt	(Varies with doping.)	±10%
Inductance	Spiral on Ferrite	10 uh Q 50	10C MA		±10%
Capacity	Junction	1000pf Voltage Variable	10-100v		±10%
Capacity	Glass SiO_2	200pf D.F. .5%	100v		±10%
Diode	Hi-speed	2 nsec	10ma 1v		

Element Function	Type	Range	Current Voltage or Power	Temperature Coefficient	Tol.
Transistor	Hi Freq. NPN	800 MC f_t	.01-10 MA		
Transistor	Star NPN	400 MC f_t	.1-500 MA		
Zener	Any	6-30v	1/2 watt max.	Varies with voltage.	10%

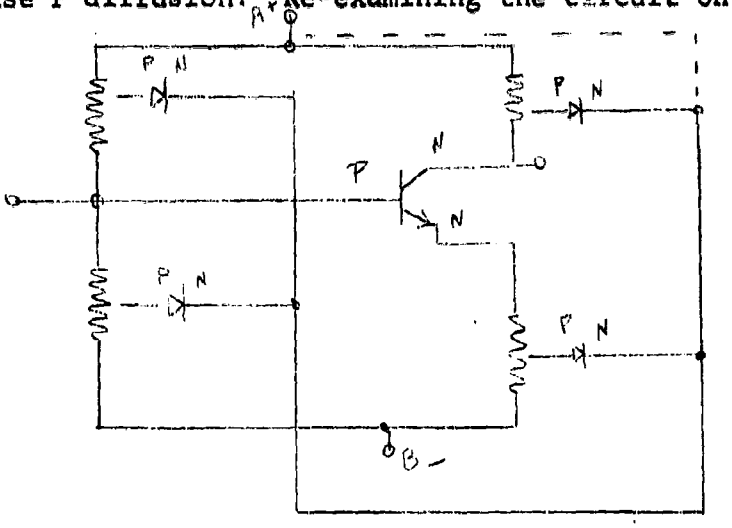
As can be seen from the chart, integrated circuits impose some restrictions on circuit design. In many cases additional external components will be required to perform complete circuit functions.

The basic insulators in integrated circuits design are the thin film oxide (SiO_2) and the back biased junction. Two junctions may be placed in series to insure isolation regardless of applied voltage:

As the first example of integrated circuit design consider the amplifier shown below.

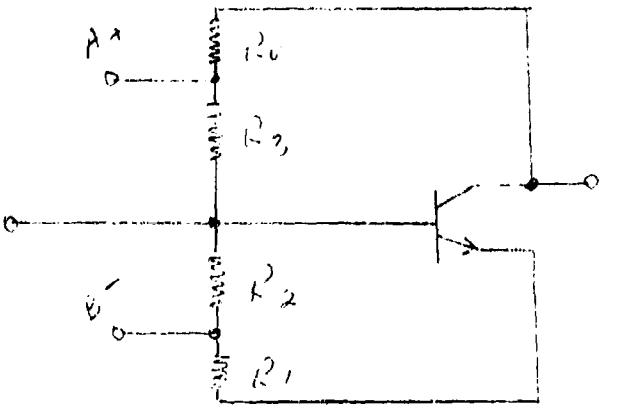


In this example all of the resistors are convenient values for the base P diffusion. Re-examining the circuit on this basis:



It is apparent that all resistors can be on a common N substrate and they must be connected to the positive terminal A to insure that the diodes will be back biased.

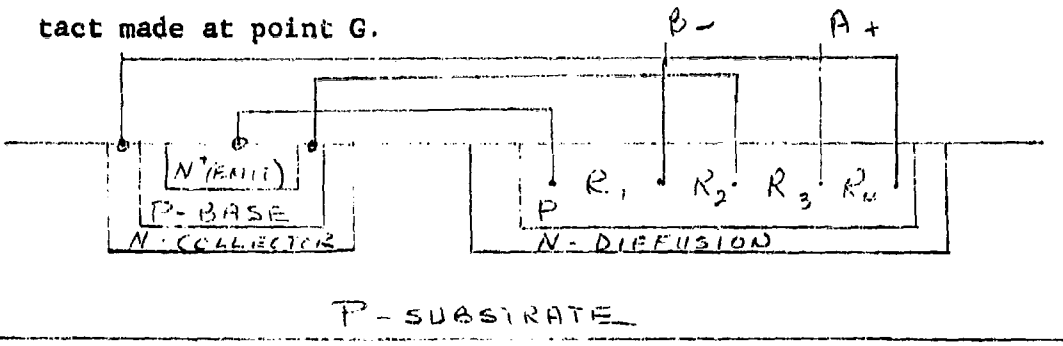
Further examination shows that the resistors are really in series and the circuit may be re-drawn as shown below:



Since P diffusion is being used for the resistors, some method must be used for separating the P silicon from the N

collector of the transistor point D.

The problem is solved with the N substrate and ohmic contacts DC and EF. The transistor base contact to the resistor can be a continuation of the base diffusion with an ohmic contact made at point G.



Following the evolution of the several steps for integrated circuit design, various circuits comprising the 120 Mc Transceiver are within the Stage 3 and Stage 4 design status.

In the stage 3 developments, several of the amplifier and other stages are under actual construction, utilizing the multi-chip approach. In these designs, the first effort will consist in packaging complete circuit units individually.

Such a circuit unit will include, say, a complete amplifier stage with transistor, all resistors, all by-pass and coupling capacitors, and when required, the AGC feed line and filter.

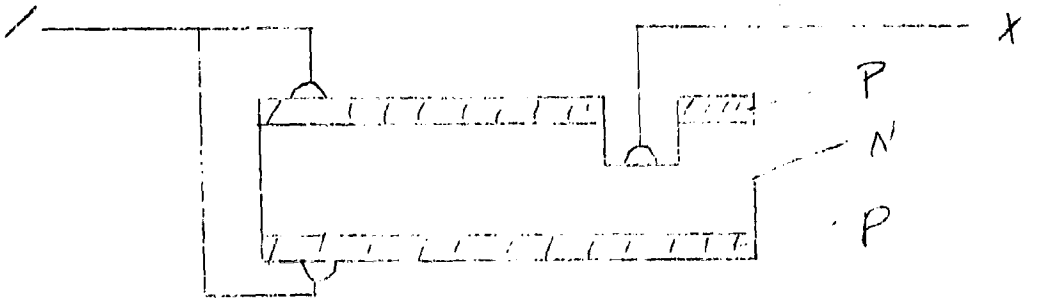
The components to be used, as described in a listing in the last report, are diffused resistors, PN junction capacitors, and high frequency NPN transistors (800 Mc f_T). These will be, in some cases, combined with thin film resistors, capacitors, and conductors, either on the ceramic substrate, or in Stage 4 fabrications, on the silicon block.

Zener diode junctions, readily available in a wide range of sizes and dopings are used as capacitances. In cases where a capacitance larger than that obtainable from the largest standard 135 mil diameter die is required, special dies, up to

180 mils in diameter may be cut from the diffused material. This diameter is approximately the maximum size which can be conveniently located within the present 10-pin header.

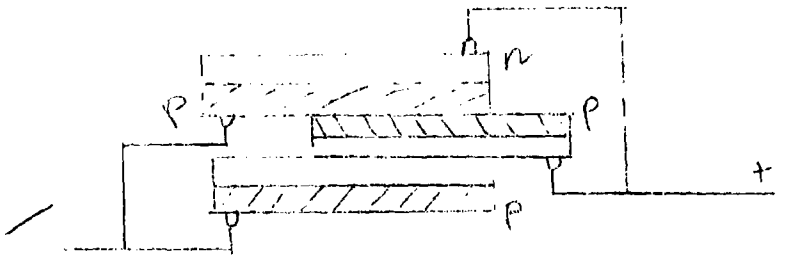
Such a diode in the lowest available resistivity diffusion, would have a capacity of approximately 33,000 pf or .033 ufd, at a working voltage up to about 5 volts.

It has been proposed to evaluate the possibilities of sandwich dies. Zener diode dies are fabricated starting with either N or P type substrate,and diffusing in layers of the opposite type which appears on both sides of the wafer. In zener diode fabrication, one of these junctions is lapped off, leaving a single PN junction. It is proposed to retain the original double diode,and by means of masking and etching techniques to establish an ohmic contact to the central junction. This structure is shown graphically herewith.



This will double the available capacitance per unit area, providing approximately 2.6 pf/mil^2.

For even larger capacitances it is quite feasible to stack standard or special dies in parallel,



to provide practical, compact, low voltage capacitors up to

perhaps .2 ufd or more.

Some of the possibilities of forming resistors and gold conductors on the ceramic wafers are being investigated by the Solid State division. The resistors are thin film nichrome with a sheet resistivity of 100 ohms per square or higher. These are ordinarily deposited on glazed or polished ceramic substrates and are reproducible to ±5% or better, with excellent thermal characteristics.

However, because of some possible incompatibilities between glazing temperatures and moly manganese bonding, an effort will be made to evaluate the deposition parameters on the unglazed wafers.

5.2 Compatible Diffused Resistors

A large number of diffused resistors were made to develop process control technology. These resistors will be used for reliability studies as well as breadboarding circuits for future studies. Electrical studies of the diffused resistors shows the possibilities of unique circuit application. The initial diffused resistors are P diffused into N. The next types to be made will be N diffused into P.

Initial studies of these diffused resistor structures show that a high degree of control may be maintained over the final value of resistance. There are two degrees of control involved with this particular geometry:

a) Control of sheet resistance of the diffused layer.

b) Control of final value obtained by pretesting individual components and bonding wires to appropriate points.

Control to ± 10% of a desired resistance may be obtained by controlling the value of sheet resistance of the diffused layer. The majority of these components fall to within ±10% of the target value of resistance. The sheet resistance of the diffused layer was known and bonding to appropriate points in the segmented pattern was determined by this value.

5.3 Compatible Tin Oxide Resistors

Efforts in applying the precision photolytic techniques to etching tin oxide have been successful. The segmented resistor pattern will be metallized and during the next reporting period experiments will be performed using tin oxide on top of transistors to prove compatibility. Problems with the etching of tin oxide thin films for extremely small structures have been resolved. The film has been repeatedly formed with structures of 0.0003" line width. Kodak photoresist techniques are used to mask selectively the tin oxide resistor regions. Silicon dioxide films have been deposited over the tin oxide during subsequent operations performed on the resistive element. The silicon dioxide is then selectively removed from the appropriate areas for placement of contacts, and contacts are then formed by vacuum metallization. The tin oxide films have been deposited upon silicon dioxide coated silicon slabs so that assembly of the tin oxide resistors closely parallels that of the silicon diffused resistor.

5.4 Compatible Silicon Dioxide Capacitors.

Additional quantities of silicon dioxide capacitors have been fabricated for reliability studies as well as circuit breadboarding. Motorola's work in failure mode analyses should be of great value in the reliability studies. A number of units have been placed on operating, as well as storage life tests.

All objectives set for the silicon dioxide capacitors have been met or exceeded. The objectives were as follows:

1. To obtain 0.1 pf/mil^2
2. To obtain capacitors with a low series resistance.
3. To obtain breakdown voltages exceeding 50 volts.
4. To obtain all three of the above objectives at a high yield.

The values obtained vary from .13 to .17 pf/mil^2. The breakdown voltages of these units has in every case been above 75 volts. The series resistance of these capacitors is less than 0.5 ohms.

The processes involved here are to take low resistivity silicon and form a very thin silicon dioxide layer on the silicon slab. The upper electrode of the capacitor is a vacuum-deposited layer of aluminum. The slabs are then processed in a manner similar to that of a silicon transistor.

5.5 Special Transistor for Integrated Circuits

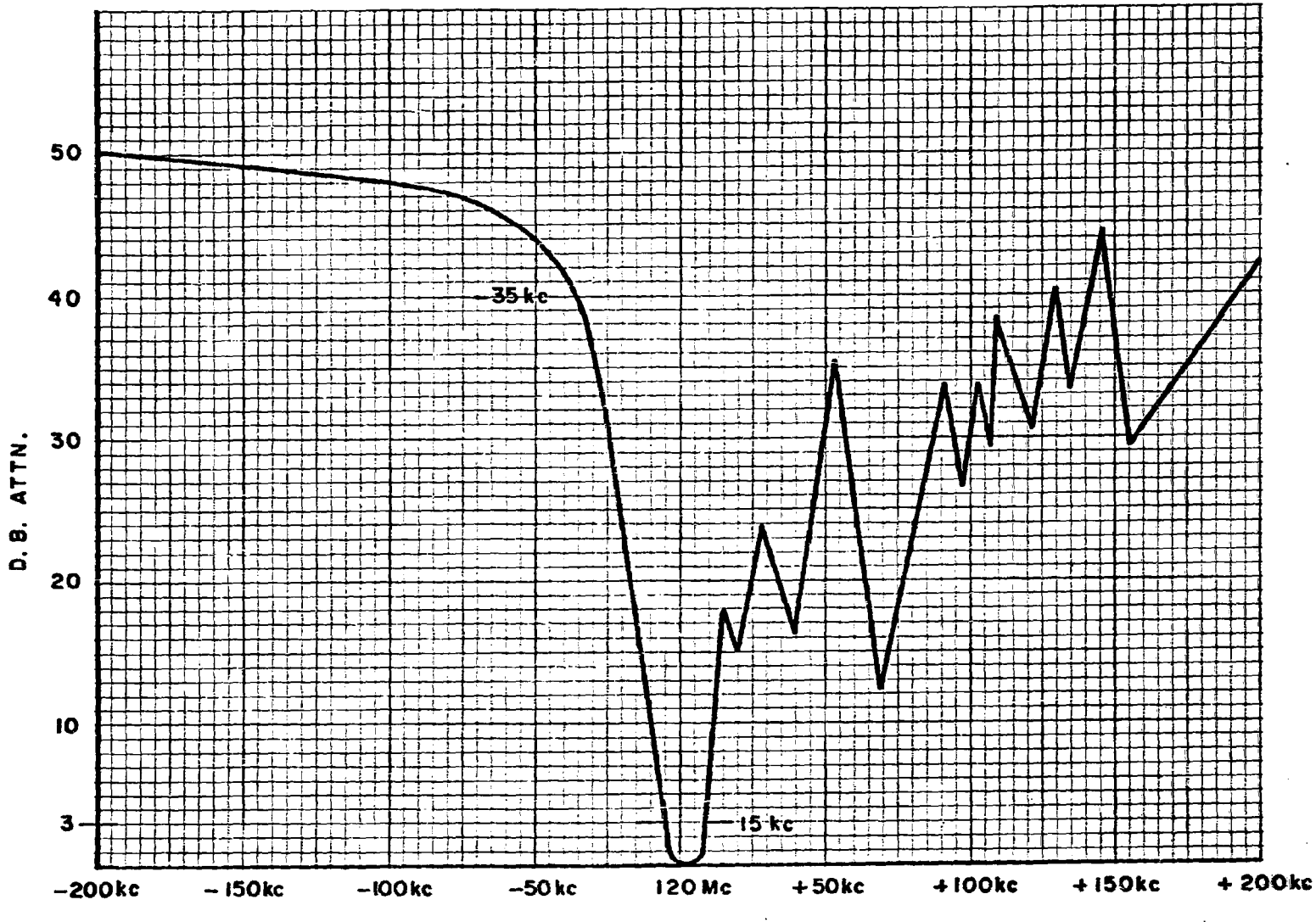
A special transistor for Integrated Circuits is being developed which is small in size to permit operation at lower currents and higher frequencies. This transistor will be used in the breadboard designs of the 120 Mc receiver. The device is currently being characterized as well as various tests in actual circuit applications.

The transistor is being designed to perform at frequencies up to 800 megacycles, with a peak in current gain at approximately 1 milliampere. The geometry will provide for ohmic collector contacts on the surface.

5.6 120 MC Transceiver Filters

Activities during the previous period were confined to the two band pass determining elements of the VHF receiver, i.e., the 120 MC and 12 MC Crystal Filters.

The first model of the 120 MC input filter was received from Motorola Chicago for evaluation. Figure 5.6.1 shows the response characteristic of the filter. Two minor shortcomings of the filter are evident. First, the spurious responses in



120 Mc XTAL FILTER

FIGURE 5.6.1

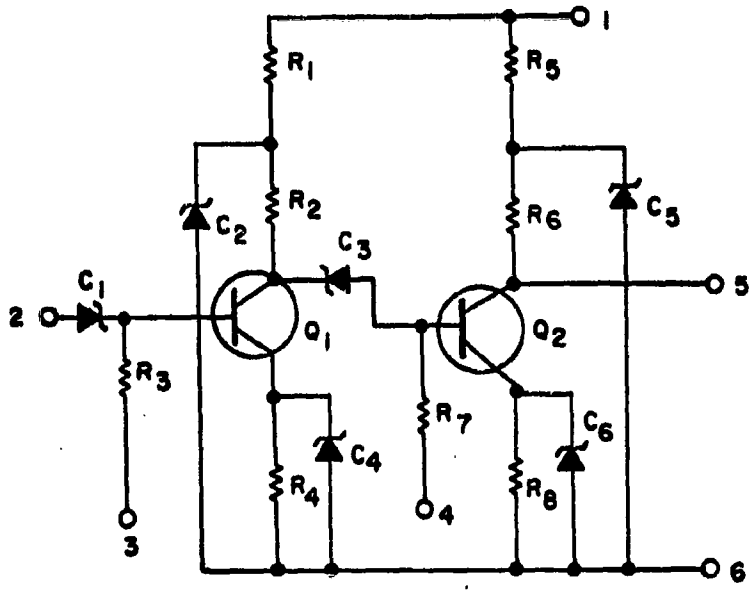


FIGURE 5.7.3

TWO STAGE CASCADE AMPLIFIER IN ONE CAN.
TWO OR MORE LAYERS WILL BE USED FOR COMPONENTS.

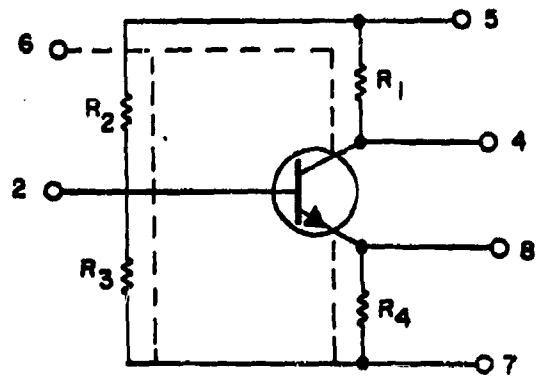


FIGURE 5.7.1

SCHEMATIC OF TWO CHIP AMPLIFIER STAGE

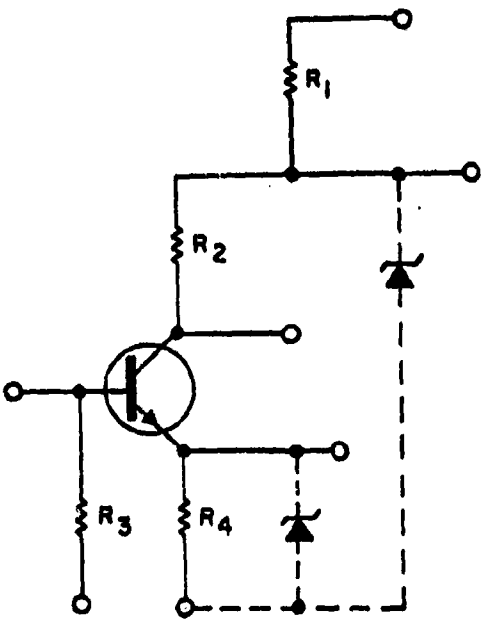


FIGURE 5.7.2

INTEGRATED AMPLIFIER CONFIGURATION. ZENER CAPACITORS WILL BE ADDED IN SUBSEQUENT MODELS.

the region of 50 KC to 200 KC above 120 MC and second the slight skew of the center frequency above 120 MC. The presence of nearby spurious response while indicating a less than ideal device should not present any system difficulties.

A few more of the more important specifications are as follows:

3 db Bandwidth	15 KC
Insertion loss at 120 MC	12 db
Input-Output impedance	100 ohms
Image Rejection	50 db

The 12 MC filter received during this period is not primarily intended as a device which will be used in future evaluations of the VHF Receiver. Rather, the unit will be used to determine what, if any, problems arise when a filter of this type is re-packaged.

In order that the filters be compatible with the remainder of the receiver, it is necessary that the unit assumes the configuration of a TO-5 package. To meet this end, the filter was designed with two important features. First, it should be readily disassembled and second,the diameter of the crystal elements used should be no larger than 0.1 inch.

In order to determine the effects of repackaging, the filter was completely evaluated prior to disassembly. In addition to the usual data on transmission characteristics, insertion loss, etc. Careful note was made of relative physical positions of various components in order to estimate the magnitude of stray capacities.

5.7 Integrated Linear Amplifiers

Two groups of typical amplifiers stages, similar to those used in the proposed receiver schematic shown in the second quarterly report, have been fabricated using separate transistor and diffused resistor chips.

The first amplifier, shown schematically in Figure 5.7.1 involves a typical base bias divider network with load and emitter resistors. Similar stages in the receiver schematic are those associated with Q2, Q6, and Q9. Since the four resistors involved

in this configuration are represented as a single tapped resistor, a single diffused resistor chip provided all of the required resistance values.

The second amplifier type, similar to Q4, Q5, Q7 and Q8 involves a resistor arrangement in which the base, emitter, and collector resistors terminate in such a way that a single resistor is not represented. In this structure, shown schematically in Figure 5.7.2, three resistor chips and one transistor chip were used. In future more complex structures, such as building two succeeding stages on one substrate, these resistors can be shared. This would result in two cascaded stages, such as Q4 and Q5, requiring only four resistor chips, and two transistors. A layout of one structure of this nature is shown in Figure 5.7.3.

The first amplifier configuration (Figure 5.7.1) has been tested and partly evaluated. Nine units were built, of which five were rejected during curve tracer tests because of open leads, incorrect resistance values, or poor transistor gain. The resistor values in the good units were measured to obtain some information on reproducibility. These measurements are recorded in Table 5.7.1. The designations are referenced to the schematic of Figure 5.7.1.

TABLE 5.7.1

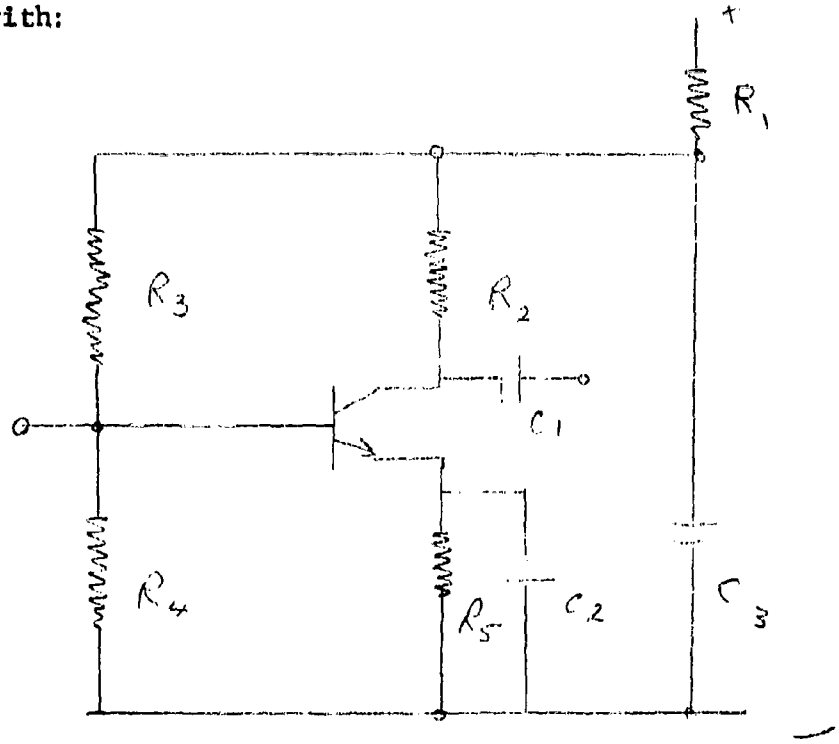
Design Value	Unit No. A	B	C	D
R_1 3K	3.0	3.7	3.0	3.5
R_2 18 K	17.0	22.0	23.0	23.0
R_3 4.7 K	4.1	4.9	5.1	7.3
R_4 2.2 K	1.9	2.1	2.3	2.5

5.8 Single Block Integrated Linear Amplifier

In the Stage 4 design area, a single silicon block amplifier circuit has been proposed, and at present is under preliminary design investigation and masking setup.

Isolation is of the back biased junction type which provides electrical isolation, but introduces parasitic capacitance which may tend to become significant in some parts of the circuit.

The conventional schematic of this stage is shown herewith:



This is a general amplifier configuration, useful at all frequency ranges. The high frequency limit of usefulness is limited by transistor characteristics (f_T, etc.) as well as by external circuit stray effects. In the case of single block integrated circuit, these strays or parasitics, may in some cases, become somewhat more significant than in conventional circuitry, thus contributing to the limitation of useful high frequency performance.

For low frequencies, the limitation is essentially the RC constants of the bypass and coupling networks.

The circuitry involved in the single block amplifier consists of essentially the same components as the conventional circuit. It is believed this amplifier will perform at 12 Mc, and may in various possible versions be used in the 12 Mc IF amplifier

stages. These could also be used in the 455 Kc IF by externally applying larger capacitors.

The construction starts with a block of P-type silicon of medium high resistivity, say 10 ohm cm. Masking, oxide etch, and diffusion techniques are utilized to build up the various areas within the surface of the block. The transistor, for example, is a quite conventional NPN-type, with an extended collector area large enough to include a P-type diffusion area. This combination provides collector coupling capacitor, C_1. Since the underlying N-type collector area is always positive with respect to the negative grounded P-type substrate, this diode is always reverse biased, having the same effect on the circuit as a shunt capacitance from collector to ground in a conventional circuit. This is the largest parasitic effect in this circuit. However, this is minimized to a relatively low value (approximately .08 pf/mil^2) because of the low substrate doping.

The resistor is formed on a diffused N-type area in the P-type substrate, with narrow P-type diffusion strips. This provides the correct resistance values for load R_2, bias R_3, R_4, and stabilization R_5, as well as RC isolation R_1, C_3. The N-type area may be tied to the most positive supply point, again providing a back bias both with (1) the substrate, and (2) all parts of the resistor chain. Capacitances from the substrate diode do not effect the circuit, but the distributed capacitance, along with the resistor, will result in some parasitic effects.

The emitter bypass capacitor is formed in another area of the substrate. If desired, this could be extended to provide a second capacitor for isolation bypass, C_3.

In the case of this capacitor, a simple way to form it would be to diffuse an N-type layer into the P substrate. This would not provide the lowest possible capacitance per unit area, because of the light doping in the substrate area. The capacitance would be about .08 pf/mil^2.

To provide the maximum capacitance, a P+ layer is first diffused into the P substrate, followed by an N+ layer. This

results in about 1.3 pf/mil^2, making the areas required for C_2 and C_3 reasonable.

Circuit connections are made by mask evaporating aluminum over the oxide glass layer. This metallization connects ohmic contacts on the various semiconductor levels with each other and with the external circuit as required.

This metallization also results in some parasitic capacitance effects. The magnitude is about .03 pf/mil^2.

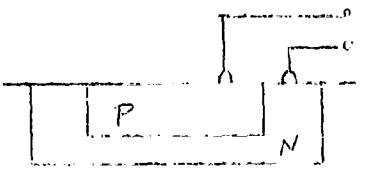
5.9 Diffused Folded Capacitor

As has been suggested in 5.7, sandwich capacitors present the possibility of essentially doubling the capacitance per unit area. This is of advantage in reducing the physical area of bypass and filter capacitors.

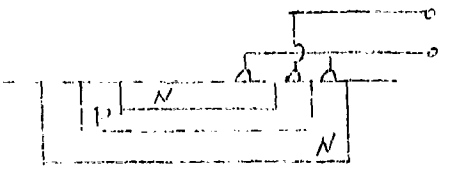
The same approach may be used to reduce parasitics in the following manner. Suppose the circuit has a given size of collector coupling capacitor, as dictated by the frequency band.

This will require a certain minimum area of the collector diffusion, which must be large enough to provide the capacitor area as well as the transistor collector and contact area.

A folded capacitor, however, will reduce the area required by the capacitor, resulting in a smaller total collector deposition area. This obviously reduces the capacitive parasitics at this point. An example of this structure is shown herewith.



NP CAPACITOR



NPN CAPACITOR

5.10 Multiple Chip Linear Amplifier Circuits

Following along the phase 3 approach already described, several amplifier and filter stages have been designed, and construction started, using the 10-pin headers, etched metallized ceramics, and individual silicon blocks (transistors, diffused resistors, diffused capacitors). Any wiring which cannot be done on the metallized ceramic is wire-bonded between the components and header posts.

A simple general layout has been worked out suitable for many of the high and intermediate frequency amplifiers in the receiver. In all cases the bypass and filter capacitors are laid down directly on the gold plated header bottom, using Au-Ge solder preforms. These capacitors are zener diode wafers, polarized with the anode down, i.e., to negative ground. The header metal is made common to ground by bridging over to pin 4.

The cathodes of these capacitors are connected to selected header posts by means of thin metallic bonding strips, or wire bonding.

The balance of the circuit is mounted to metallized areas on a scalloped ceramic. These components consist of diffused tapped resistors, transistor, and output coupling capacitor. This is mounted above the header, using ceramic spacers and post bonding for anchor.

On the immediate evaluation program, the complete circuit including all amplifiers in the 12 Mc and 455 Kc sections, will be assembled in this two level structure. Later, four level structures will be designed, which will include two or more amplifier or other stages.

6. PHOTOMECHANICAL TECHNOLOGY

During the past month, the photographic laboratory developed a technique to fabricate series of inter-related photo-masks with a minimum effort spent in preparing original art work. Using this technique a diode photomask library was prepared which makes available to the designer diode mask geometries ranging from .0005" diameter circles to .015" diameter circles on identical center dimensions which are interchangeable. It is evident that the availability of such a mask library supplies a most valuable tool for the fast evaluation of electrical parameters of diodes used in integrated circuit design.

A set of metallizing masks was completed where the concept of inter-related masks was used to prepare progressively differing mask geometries.

In addition to the masks discussed above, two mask sets for a UHF transistor and a simple flip-flop circuit were also fabricated during the past month.

This laboratory is continually improving on techniques and processes as well as personnel competence to supply photomask and other parts fabricated by photo technological methods.

7. CIRCUIT CONSIDERATIONS

7.1 V.H.F. RECEIVER

The evaluation of the breadboard version of the V.H.F. Receiver has been completed. In order that a valid comparison between the conventional components and the Integrated Circuit components which will be substituted be made, all functions of the receiver have been examined to determine gains, bandwidth, etc. For purposes of receiver evaluation, a 2 pole bandpass filter was designed and substituted for the Crystal Filter. The absence of the crystal filter is evident when examining the graph of spurious responses. The response of the image frequency (96 MC) is only 35 db below the 120 MC response.

Also, during this period, a selection of Integrated Circuit components were received. Included were a group of diffused resistors ranging in value from 820 ohm to 6800 ohm.

The 12 MC I.F. was chosen as the vehicle for the first trial substitution of Integrated Circuits components. The particular circuit function was selected for two reasons. First, the frequency of operation was high enough to be greatly effected by any unwanted parasitic elements introduced by the new components. Secondly, the range of values of capacitors and diffused resistors available closely matched the required values.

The capacitor substitution should not cause a change in performance of the I.F. amplifier; on the other hand, the effect resistors will have on the performance will have to be determined in two steps. First, direct substitution leaving the common die connection floating, and second, connecting all common points together to a source of reverse bias voltage.

To understand the reason for the two steps above, it must be remembered that the diffused resistor is in effect a distributed R-C network where the capacitor is the result of the P-N junction formed by the diffusion process. As such, the capacitor becomes a voltage sensitive parasitic element.

SENSITIVITY AND QUIETING

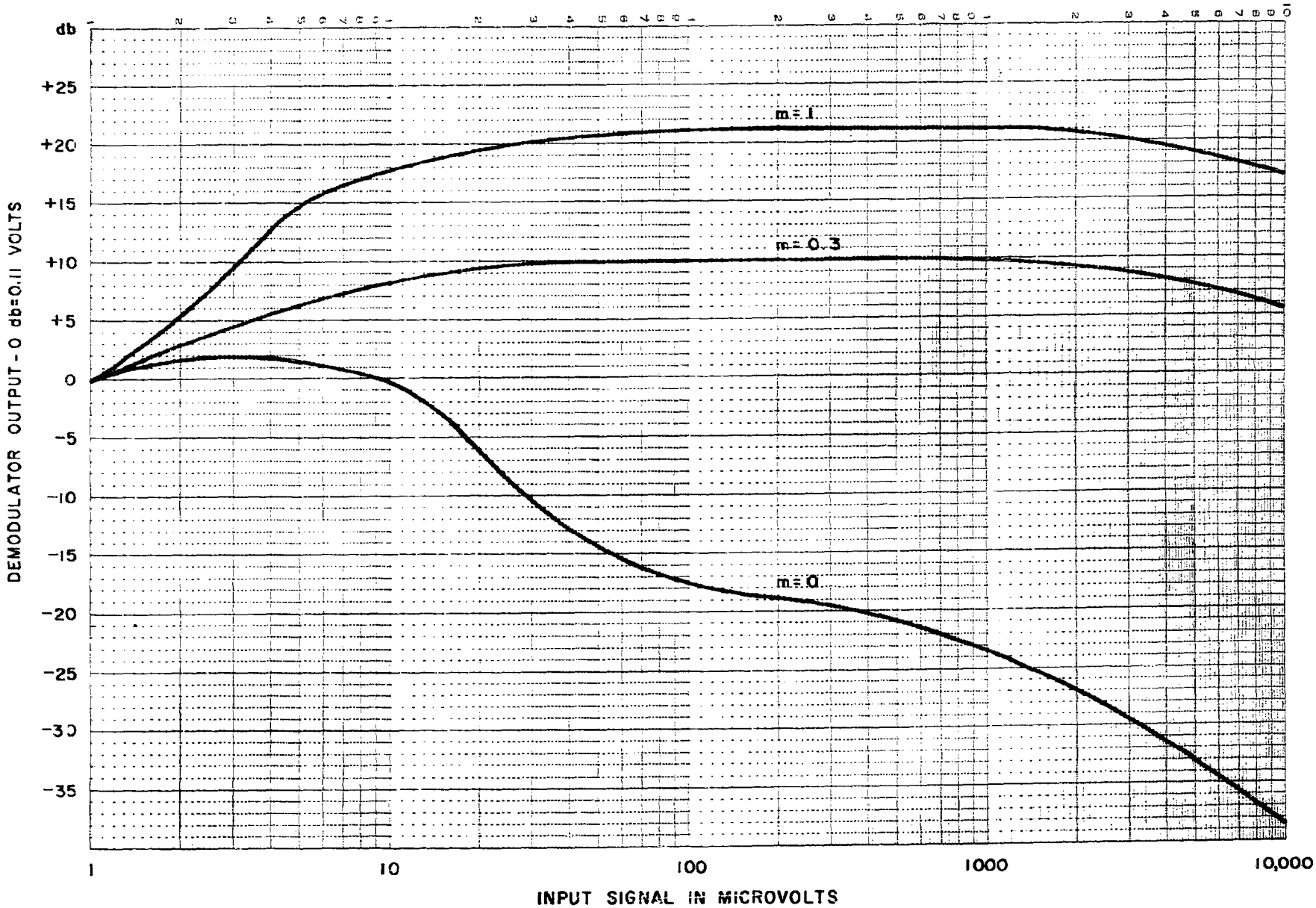


FIGURE 7.1.1

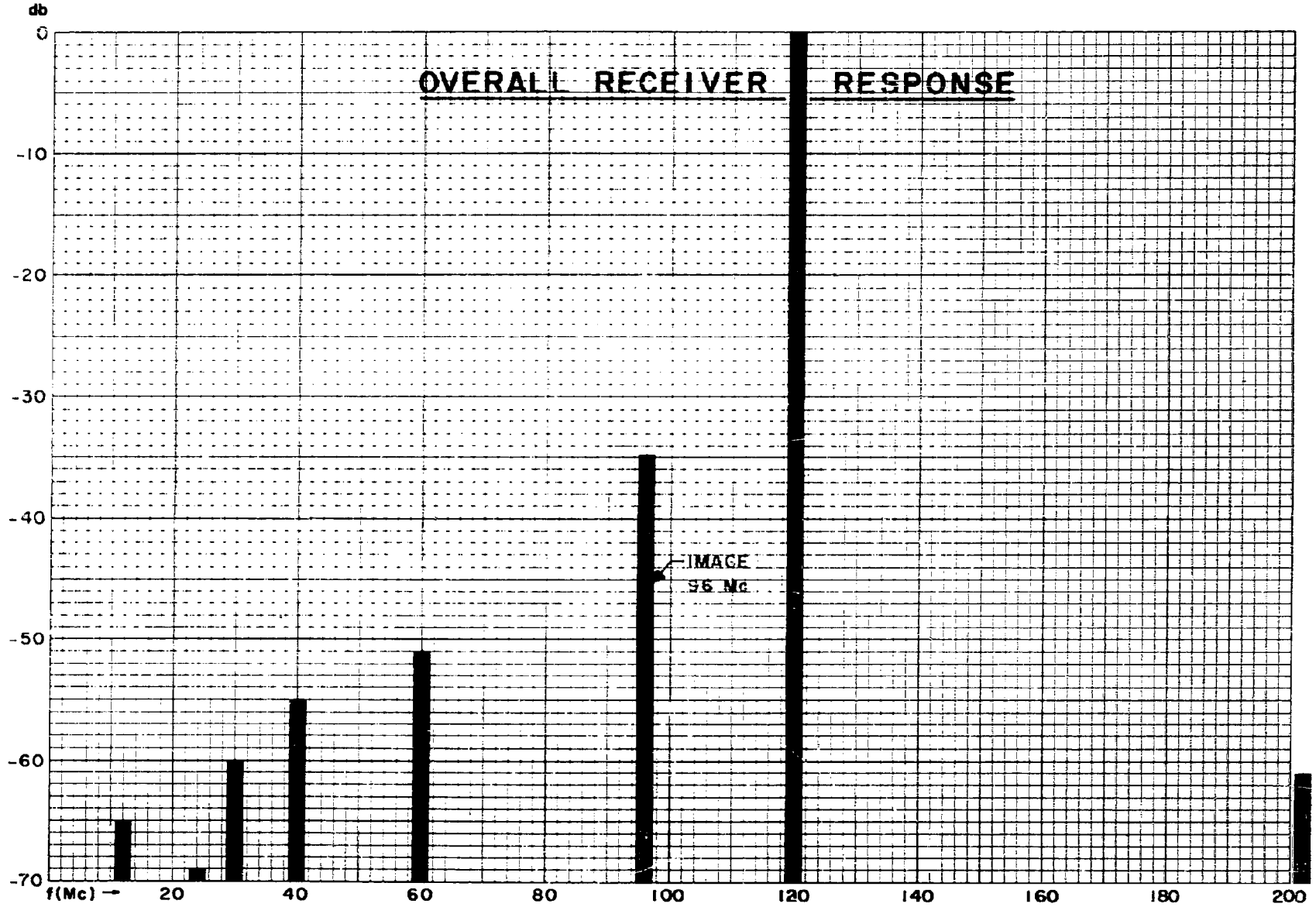

db
0
-10
-20
-30
-40
-50
-60
-70
OVERALL RECEIVER RESPONSE
IMAGE
96 Mc
f(Mc) →
20
40
60
80
100
120
140
160
180
200

FIGURE 7.1.2

12 MC CRYSTAL FILTER

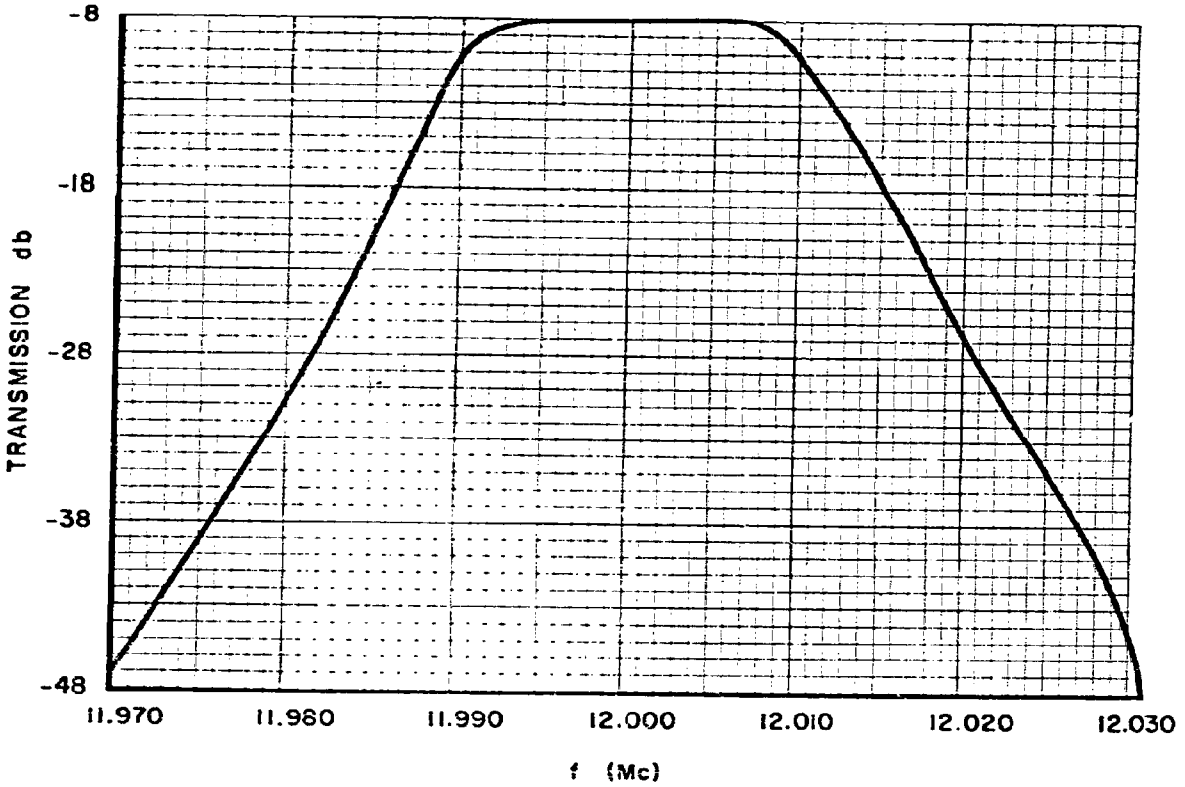


FIGURE 7.1.3

1ST IF AMPLIFIER (12 Mc)

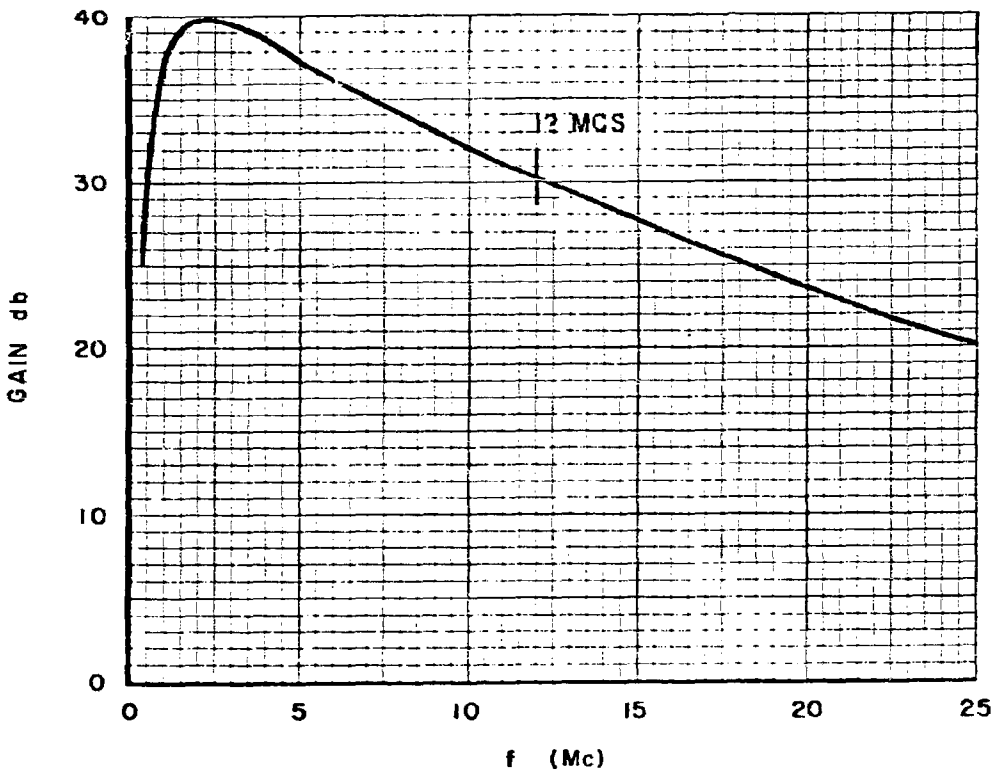


FIGURE 7.1.4

2ND IF AMPLIFIER (455 KC)

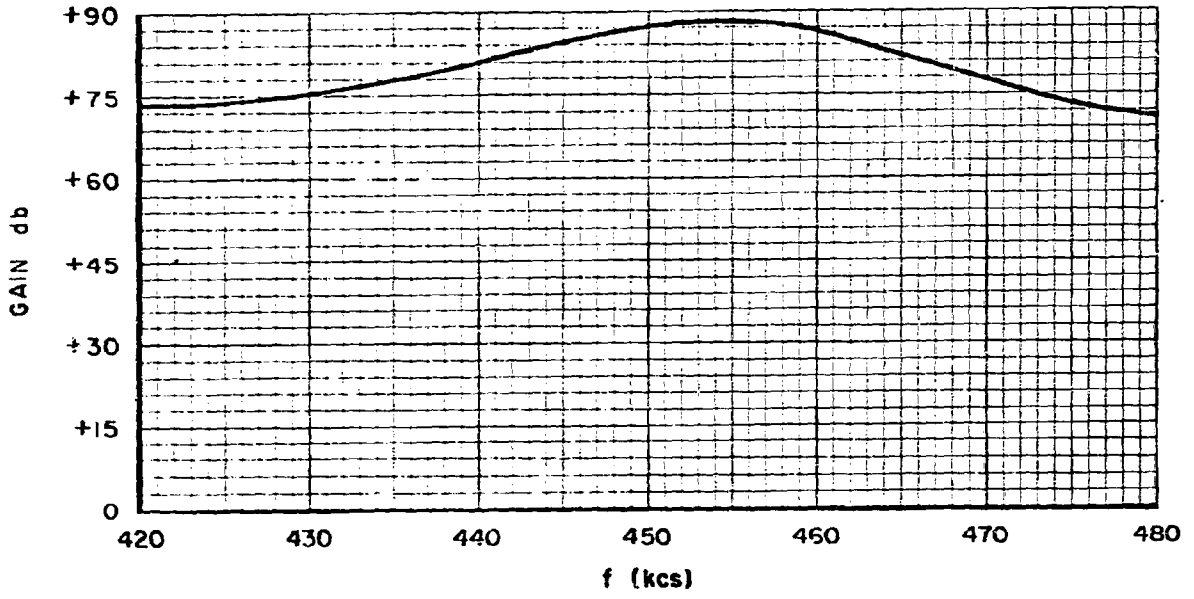


FIGURE 7.1.5

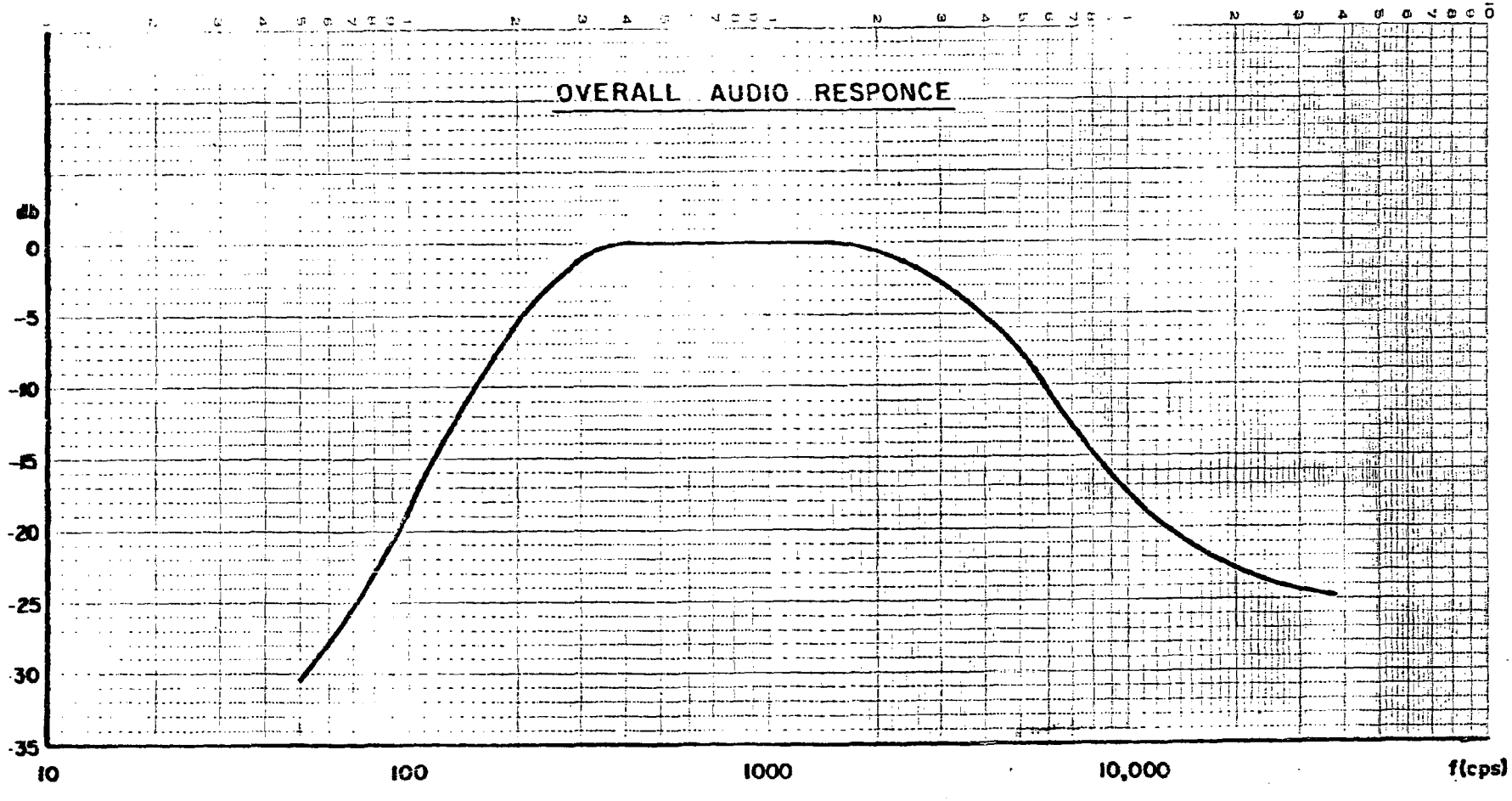

OVERALL AUDIO RESPONCE
db
0
-5
-10
-15
-20
-25
-30
-35
10
100
1000
10,000
f(cps)

FIGURE 7.1.6

The first step mentioned above has been completed; that is, the capacitors and diffused resistors have been put in breadboard. Re-evaluation of the Receiver System and of the I.F. Amplifier did not indicate a change in performance after the substitution. The results of connecting the common points to a reverse bias supply will be investigated further.

Performance Curves - Results of the receiver evaluation for the major tests performed are described below:

Figure 7.1.1 shows the sensitivity and quieting characteristics for modulation indices of 1.0, 0.3 and 0. For m = 0 a slight increase in noise output occurs as the input signal level is increased from zero. This is thought to be caused by an increase in demodulator efficiency with an increase in signal level. At an input level of 6 to 8 microvolts, the A.G.C. effect begins to override the increasing detector efficiency and the noise level drops.

Figure 7.1.2 shows all receiver responses greater than 70 db below the desired signal in the frequency range indicated.

Figure 7.1.3 shows the 12 mc. crystal filter transmission vs. frequency. The insertion loss is indicated at 8 db with a 3 db bandwidth of 20 kc.

Figure 7.1.4 shows the first I.F. amplifier gain characteristic.

Figure 7.1.5 shows the second I.F. amplifier (455 kc) gain characteristic. A degree of selectivity is provided at 455 kc in order to discriminate against the broad band noise generated in the 12 mc I.F. amplifier.

Figure 7.1.6 shows the overall receiver audio response obtained by receiving a constant amplitude signal of varying modulation frequency. The output was measured across the speaker terminals. The 3 db response frequencies are 250 and 3300 cycles/second.

7.2 120 MCS. TRANSMITTER

Circuit Description - A circuit schematic of the 120 mc transmitter is shown in Figure 7.2.1.

Oscillator - The oscillator is a crystal controlled Colpitts type oscillator operating at a frequency of 120 mcs. The a-c configuration is common-base. Bias stability is gained by a common collector D.C. configuration.

A fifth overtone crystal operating in the series resonant mode provides the feedback path and frequency control. A small inductance in parallel with the crystal neutralizes holder capacitance.

The emitter of the oscillator is direct coupled to the base of the modulated amplifier and supplies the D.C. bias for the modulated amplifier.

Modulated Amplifier - The modulated amplifier is a class A R.F. amplifier stage direct coupled to the oscillator and coupled to the output stage by an impedance matching network. An impedance matching network of the "Tap" network form was chosen to allow the use of the inductance as a path for the D.C. Collector circuit thereby minimizing the number of inductors required.

Audio Modulation is applied to the emitter of this amplifier stage and modulates the R.F. signal by changing the gain of the stage.

Class "B" Output Stage - The output stage is a grounded emitter amplifier biased slightly beyond Class "B" by keeping both base and emitter at ground potential. A diode is used to clamp the base during the negative half cycle of the R.F. input and provide a path for the D.C. base current. A "Tap" network is used to couple the output amplifier to the antenna.

Modulator - A cascaded two stage emitter follower or "Darlington" amplifier is used to modulate the emitter of the modulated amplifier. The two-stage emitter follower is necessary to transform the approximately 100 ohm emitter impedance of the modulated amplifier to an impedance compatible with available diode coupling capacitors. The level of

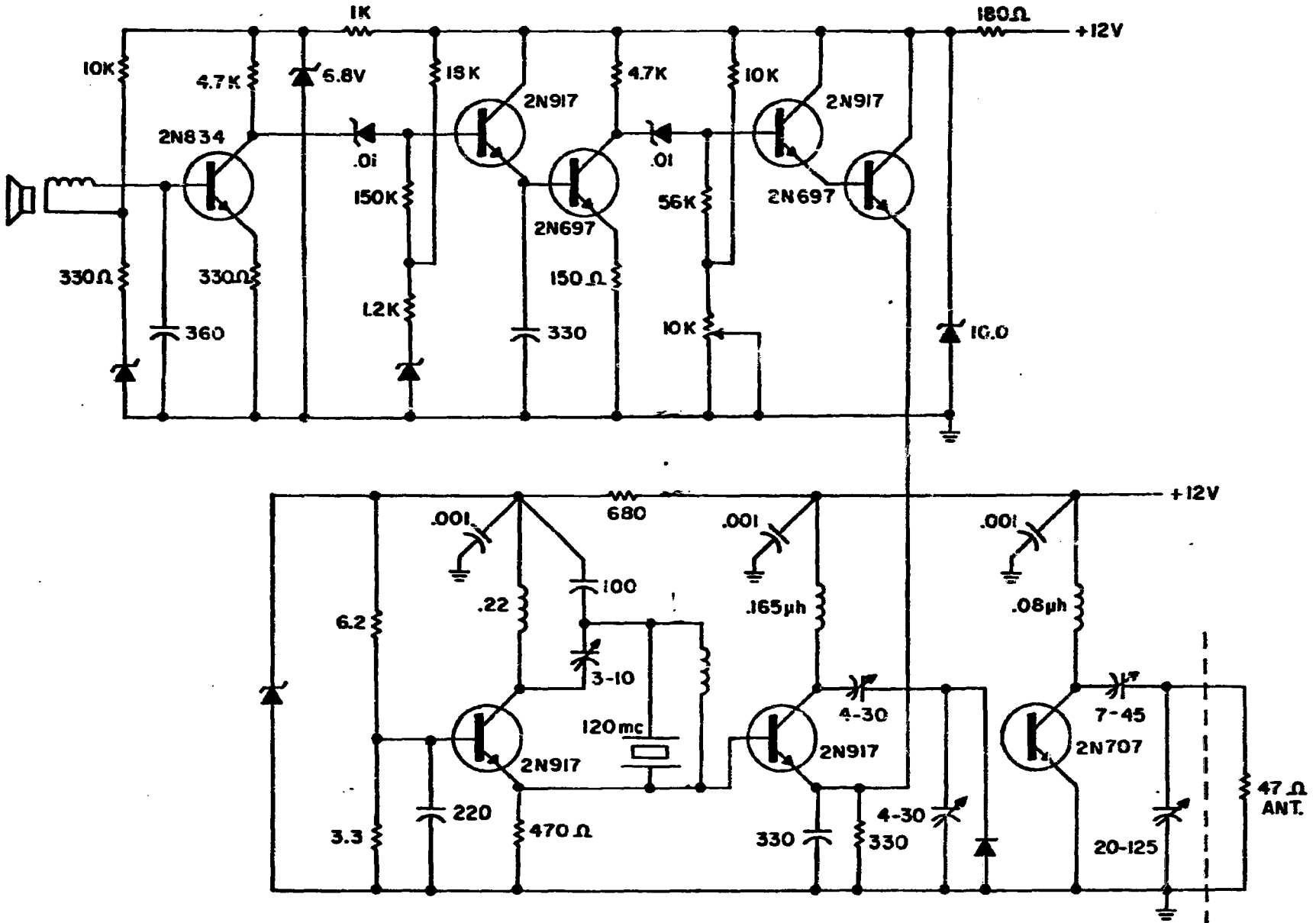


FIGURE 7.2.1
120mc TRANSMITTER

the unmodulated carrier is set by adjusting the base current of the first emitter follower.

Audio Amplifier - The audio amplifier consists of a common emitter stage followed by a common collector-common emitter pair. A magnetic microphone is connected in series with the base of the first transistor and furnishes a path for the D.C. bias current. Sufficient gain for full modulation of the transmitter is set by initial selection of the emitter resistor.

Performance Description: Power Output: A maximum power output of 85 mw. was obtained at 120 mcs. An increase in output will probably require an increase in supply voltag change in transistor type or paralleling of output transisto

Stability: The stability of the R.F. carrier level is very poor. The unmodulated carrier level is a function of:

a) Oscillator output
b) Modulated amplifier gain
c) Output amplifier gain
d) Oscillator bias stability
e) Modulator bias stability

The major cause of level instability is believed to be variation in the 120 mc oscillator output. The varying load the modulated amplifier presents to the oscillator probably contributes to this instability. Stray feedback fro the power amplifier to the oscillator is another contributing factor.

Modulation: 100% modulation was obtained in the sense that the carrier could be reduced to zero by the modulating signal. Downward modulation is fairly linear while upward modulation becomes very nonlinear at about 80% of maximum output. Low distortion can only be obtained by limiting the degree of modulation or correcting the nonlinearity by some scheme such as modulation feedback.

UNCLASSIFIED